FIG. 1

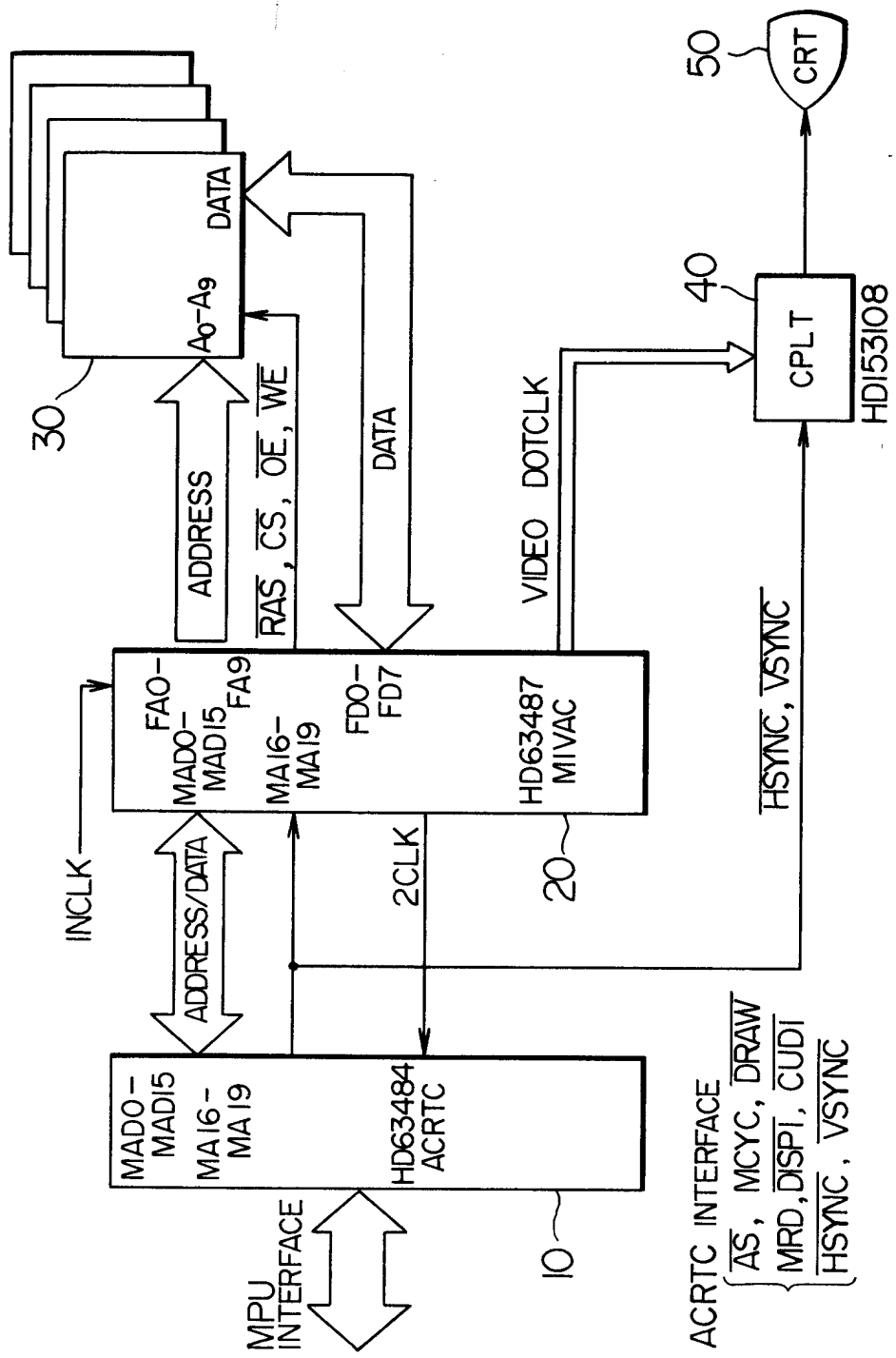


FIG. 2

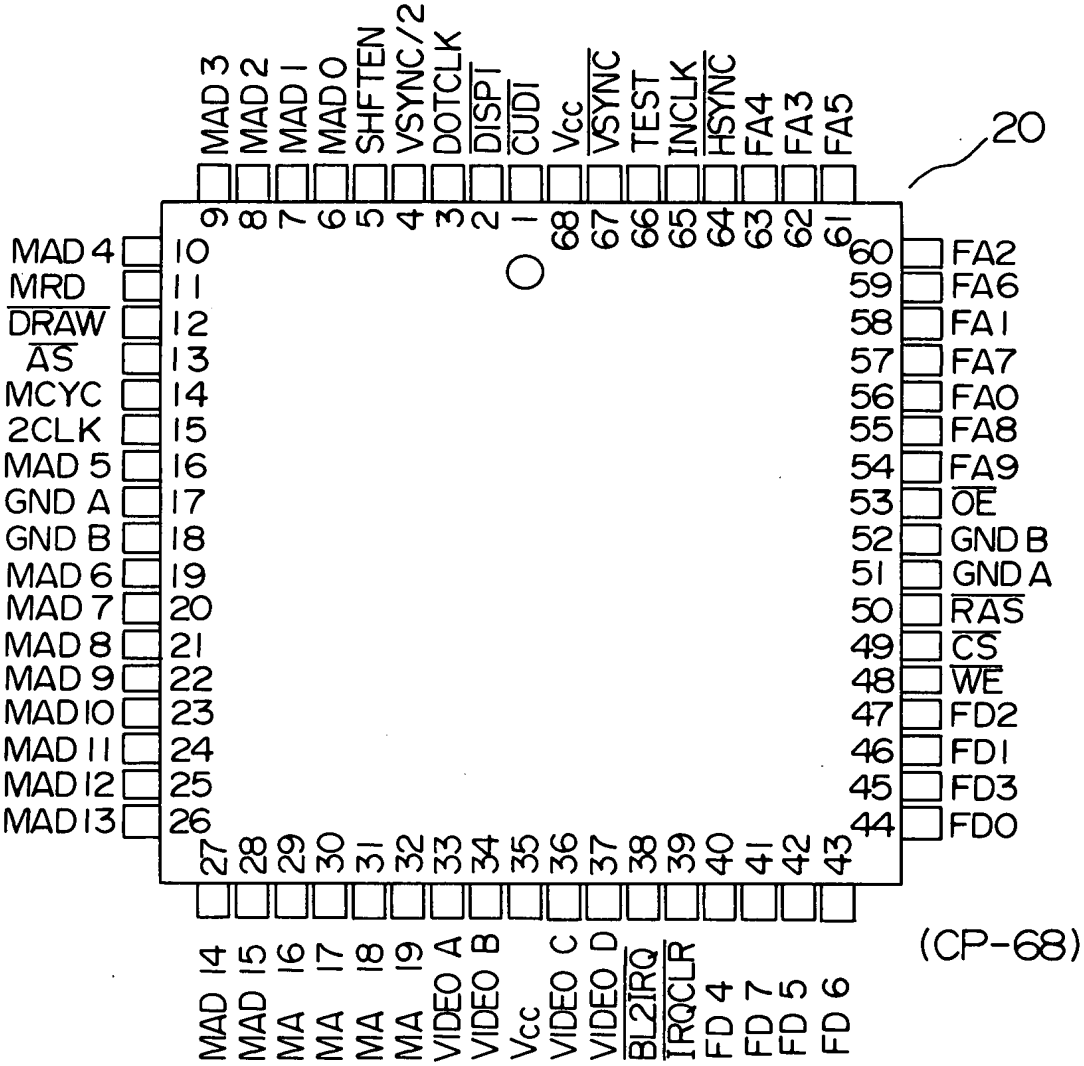


FIG. 3a

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/ OUTPUT	FUNCTION
POWER SUPPLY	35,68	Vcc	—	+ 5V IS SUPPLIED.
	17,18 51,52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC, NAMELY, HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE.
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. MCYO INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	$\overline{\text{DRAW}}$	INPUT	$\overline{\text{DRAW}}$ SIGNAL FROM ACRTC IS INPUTTED. $\overline{\text{DRAW}}$ INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. $\overline{\text{DRAW}}$ IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	$\overline{\text{AS}}$	INPUT	$\overline{\text{AS}}$ SIGNAL IS INPUTTED FROM ACRTC $\overline{\text{AS}}$ INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	$\overline{\text{HSYNC}}$	INPUT	$\overline{\text{HSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF $\overline{\text{HSYNC}}$ = "LOW" AND $\overline{\text{DRAW}}$ = "HIGH", IF AS PULSE IS RECEIVED, $\overline{\text{CS}}$ BEFORE RAS REFRESH OPERATION IS CARRIED OUT.
	67	$\overline{\text{VSYNC}}$	INPUT	$\overline{\text{VSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. RECEIVED $\overline{\text{VSYNC}}$ IS DIVIDED BY TWO SO AS TO OUTPUTTED AS VSYNC/2 SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	$\overline{\text{DISP 1}}$	INPUT	$\overline{\text{DISP 1}}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{\text{DISP 1}}$ INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	$\overline{\text{CUD1}}$	INPUT	$\overline{\text{CUD 1}}$ SIGNAL IS INPUTTED FROM ACRTIC. $\overline{\text{CUD 1}}$ IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6–10 16 19–28	MAD0 –MAD15	INPUT/ OUTPUT	MOD0–MAD 15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC = "LOW", AS DATA INPUT/ OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC = "HIGH".
	29-32	MA16– MA19	INPUT	FRAME BUFFER ACCESS ADDRESS MA16 – MA19 IS INPUTTED FROM ACRTC.

APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

FIG. 3b

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	$\overline{RAS}$	OUTPUT	$\overline{RAS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	$\overline{CS}$	OUTPUT	$\overline{CS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	$\overline{WE}$	OUTPUT	$\overline{WE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	$\overline{OE}$	OUTPUT	$\overline{OE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	56,58 60,62 63,61 59,57 55,54	FA0-FA9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF0-VCF3 AND VMD0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FD0-FD7	INPUT/OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD0-FD3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD0-FD7 ARE USED.
CRT DISPLAY INTERFACE SIGNAL	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 AND 4. DIVISION RATIO IS SET DEPENDING ON VCF0-VCF3 OF ATTRIBUTE CODE.
	33,34 36,37	VIDEO A -VIDEO D	OUTPUT	VIDEO A-DSIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY SHIFTEN OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE VCF0-VCF3.
	5	SHIFTEN	OUTPUT	SHIFEN INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, $\overline{DISP1}$ FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, $\overline{DISP1}$ IS ECONGATED BACKWARD BY TWO SYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSYNC.2	OUTPUT	VSYNC/2 SIGNAL IS INPUTTED TO ACRTC. $\overline{VSYNC}$ IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
OTHERS	38	$\overline{BL2IRQ}$	OUTPUT	$\overline{BL2IRQ}$ IS SET BY BLINK2(MA19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK2 IS AT "HIGH" LEVEL, $\overline{BLINK2}$ IS SET TO "LOW" LEVEL.
	39	$\overline{IRQCLR}$	INPUT	$\overline{IRQCLR}$ SIGNAL IS USED TO CLEAR $\overline{BL2IRQ}$ SIGNAL. WHEN "LOW" IS INPUTTED TO $\overline{IRQCLR}$, $\overline{BL2IRQ}$ IS CLEARED TO "HIGH" LEVEL.

FIG. 4

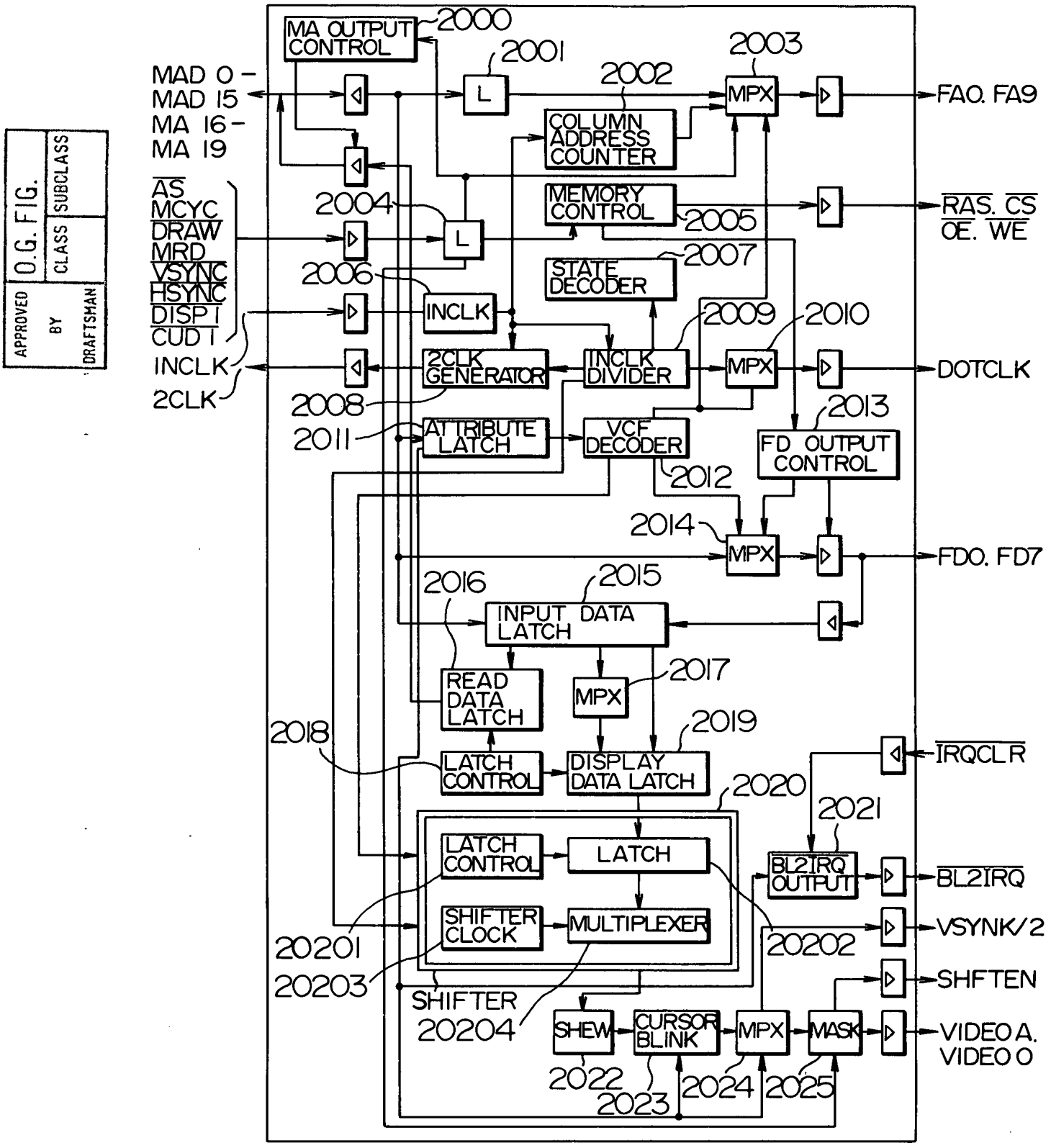


FIG. 5a

1-CHIP MEMORY

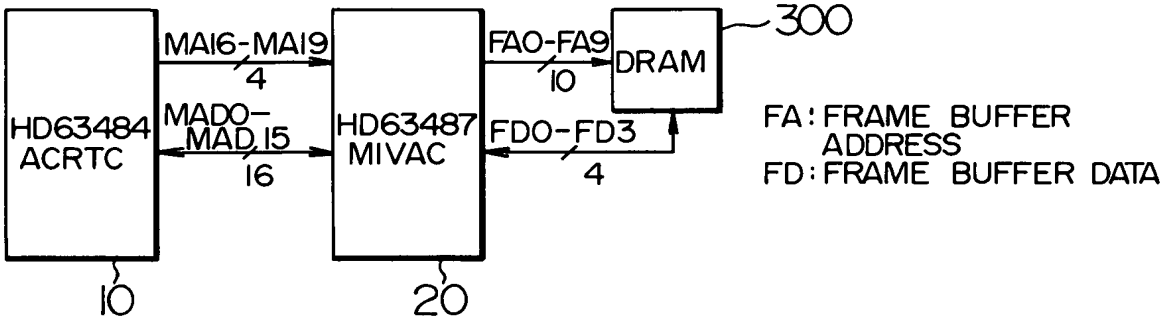


FIG. 5b 2-CHIP MEMORY

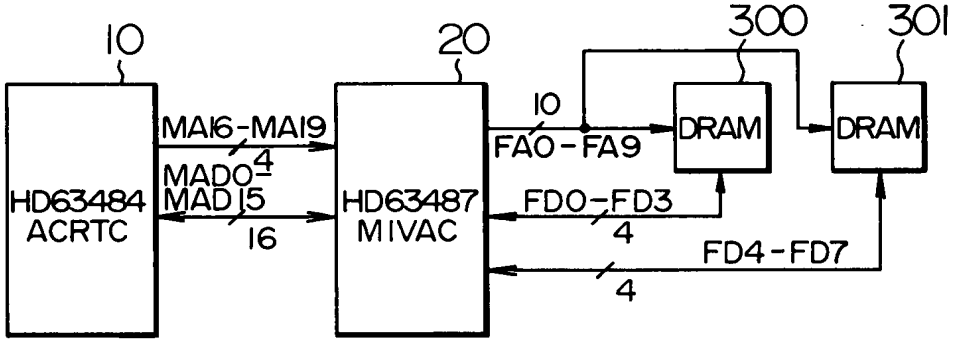


FIG. 5c

4-CHIP MEMORY

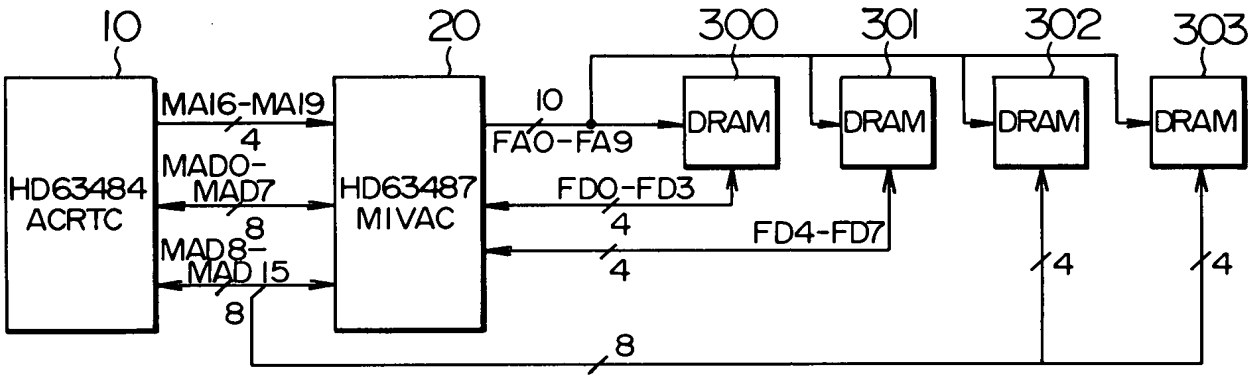


FIG. 6

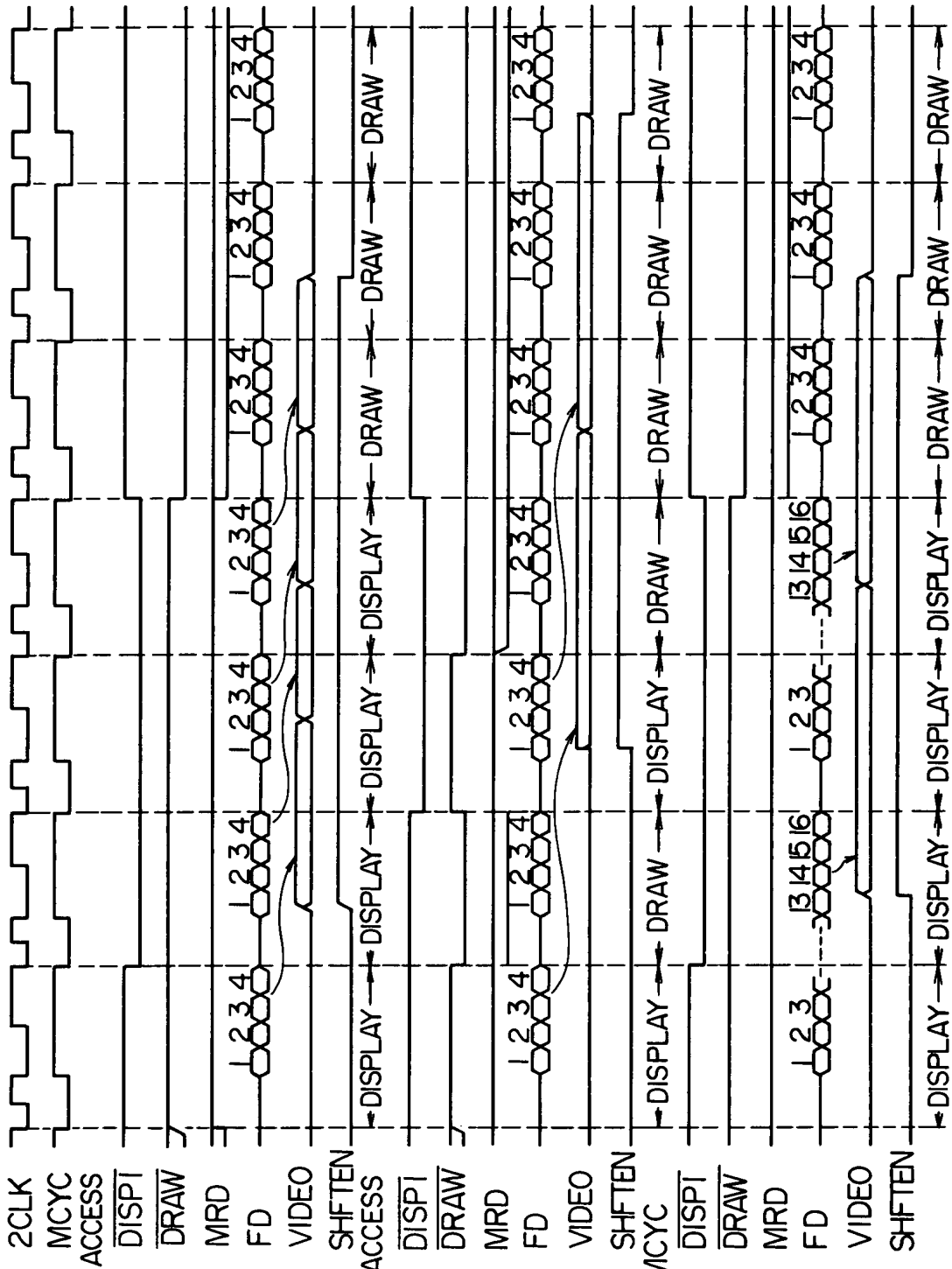


FIG. 7

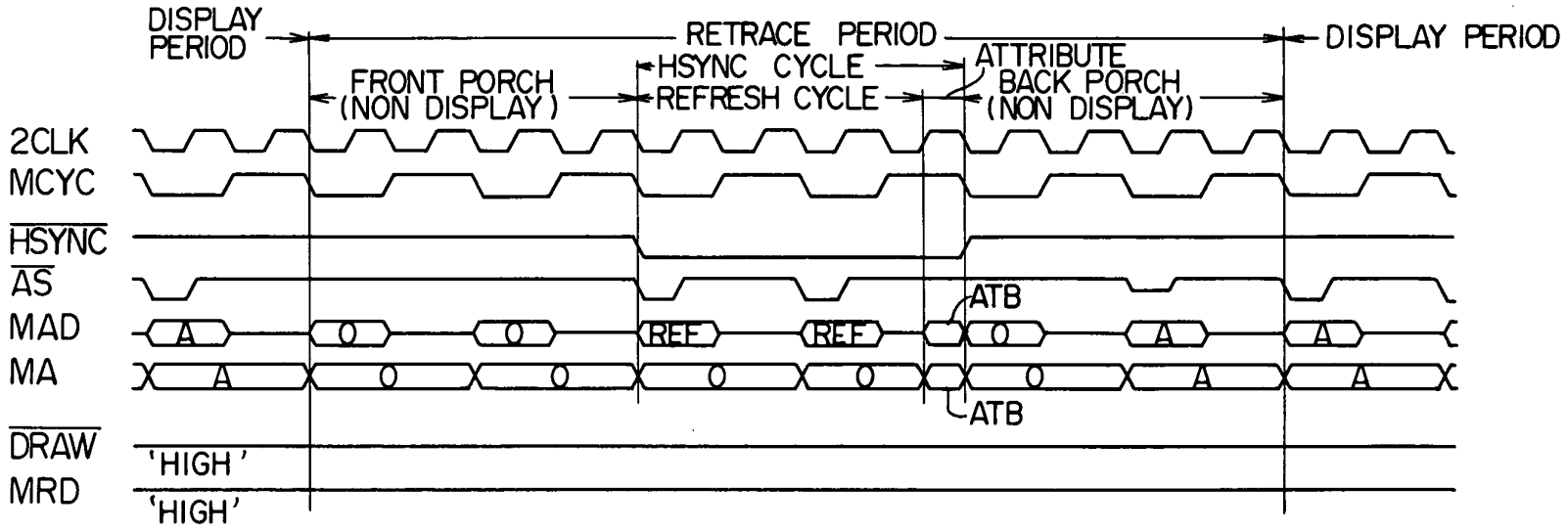
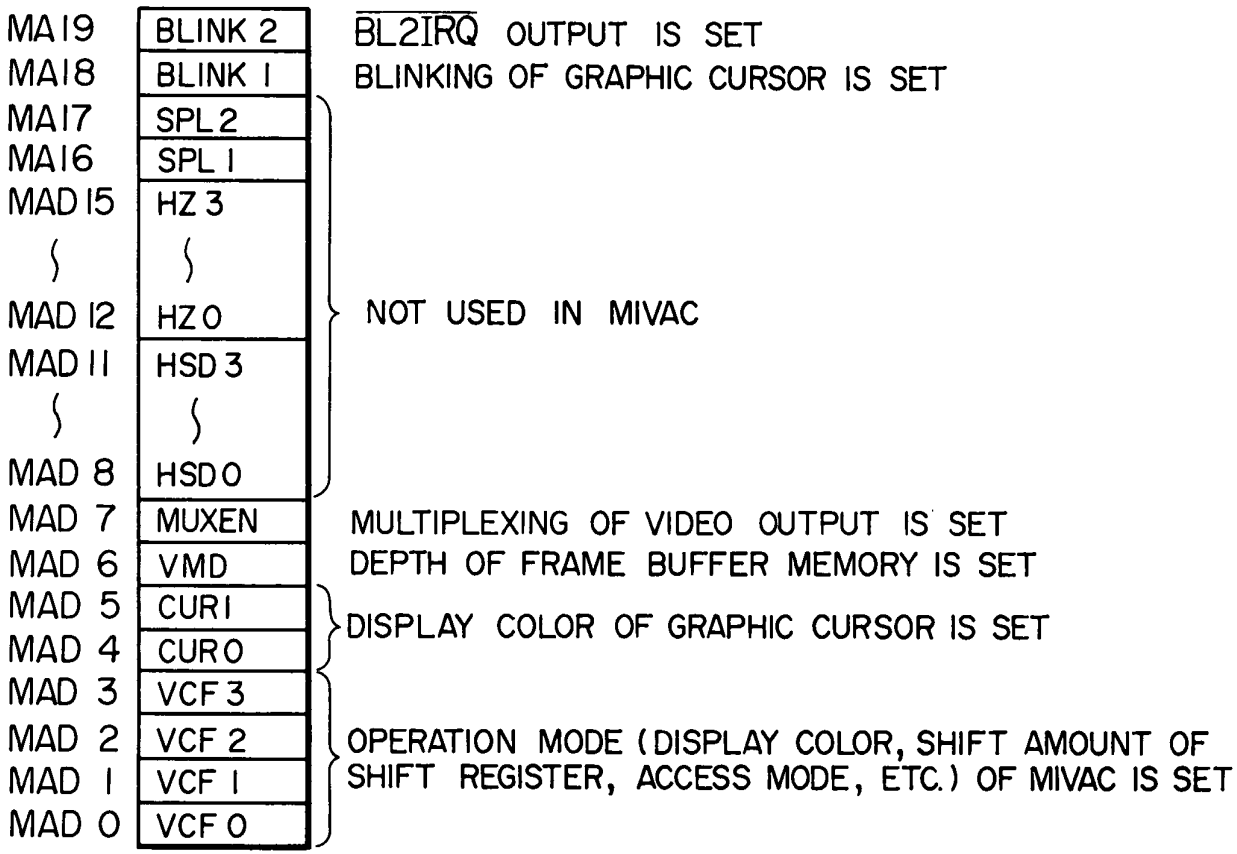


FIG. 11

CUR I	CUR O	CURSOR DISPLAY COLOR
0	0	BLACK (VIDEO A - VIDEO D = 0)
0	1	WHITE (VIDEO A - VIDEO D = 1)
1	0	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D
1	1	COLOR REVERSION FOR EACH BIT OF VIDEO A-VIDEO D (VIDEO D IS KEPT UNCHANGED)

APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

FIG. 8



APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

FIG. 9

MODE	CRT SCREEN LAYOUT EXAMPLE (DOTS X RASTER)	MAXIMUM FRAME BUFFER CAPACITY (BYTES)	ACRTC OPERATION FREQUENCY (MHz)	MEMORY ACCESS SPEED	HIGH-SPEED DRAWING	NUMBER OF MEMORIES	COLOR/GRADATION	SHIFT AMOUNT (BITS)	MAXIMUM DOT CLOCK FREQ. (MHz)
0	640×200, 350, 400, 480	512K/128K	4.13	480 ns/4ACCESSES	—	1		16	33
1	640×200, 480×240, 320×200, 240						4	8	16.5
2	320×200, 240 266×192						16	4	8.25
3	640×200, 350, 400, 480	1M/256K				2	4	16	33
4	640×200, 480×240, 320×200, 240						16	8	16.5
5	640×200, 350, 400, 480	2M/512K				4		16	33
6	640×200, 480×240, 320×200, 240	512K/128K			○	1			16.5
7	320×200, 240 256×192,						4	8	8.25
8	640×200, 350, 400, 480	1M/256K				2		32	33
9	640×200, 480×240, 320×200, 240						4	16	16.5
A	320×200, 240 256×192						16	8	8.25
B	640×200, 350, 400, 480	2M/512K				4	4	32	33
C	640×200, 480×240, 320×200, 240						16	16	16.5
D	640×200, 350, 400, 480	512K/128K		960ns/16ACCESSES	—	1	4	32	33
E	640×200, 480×240, 320×200, 240						16	16	16.5
F	640×200, 350, 400, 480	1M/256K				2		32	33

FIG. 10

MODE	DOT CLOCK FREQUENCY
0, 3, 5, 8 B, D, F	33MHz ~ 11MHz
1, 4, 6, 9 C, E	16.5MHz ~ 5.5MHz
2, 7, A	8.25MHz ~ 2.75MHz

FIG. 12

VMD	MEMORY CHIP EMPLOYED
0	256K × 4BIT DRAM
1	1M × 4BIT DRAM

FIG. 13

MUXEN	VSYNC/2	VIDEO A	VIDEO B
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

FIG. 14

BLINK 1	GRAPHIC CURSOR DISPLAY
0	NOT DISPLAYED
1	DISPLAYED

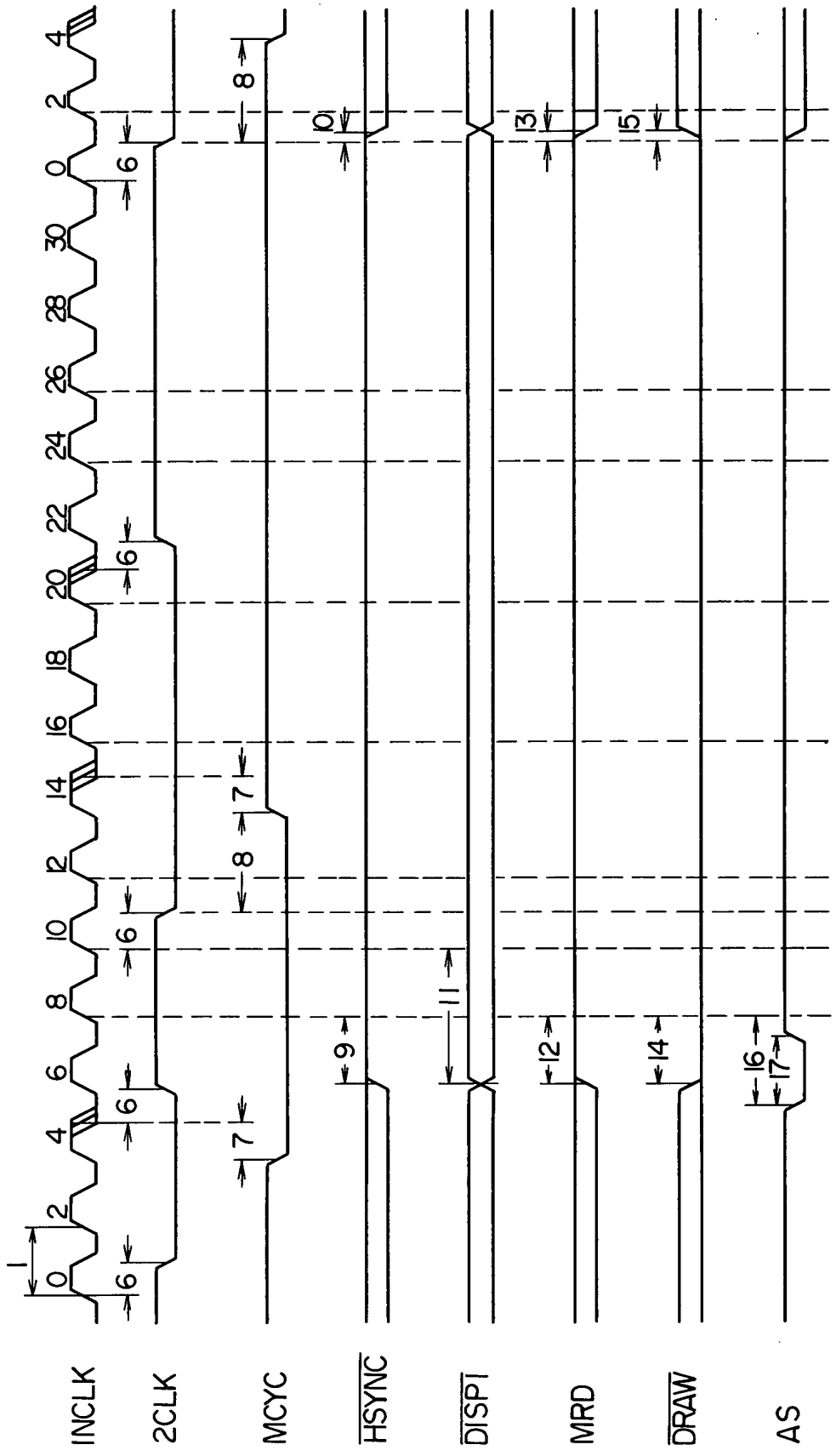
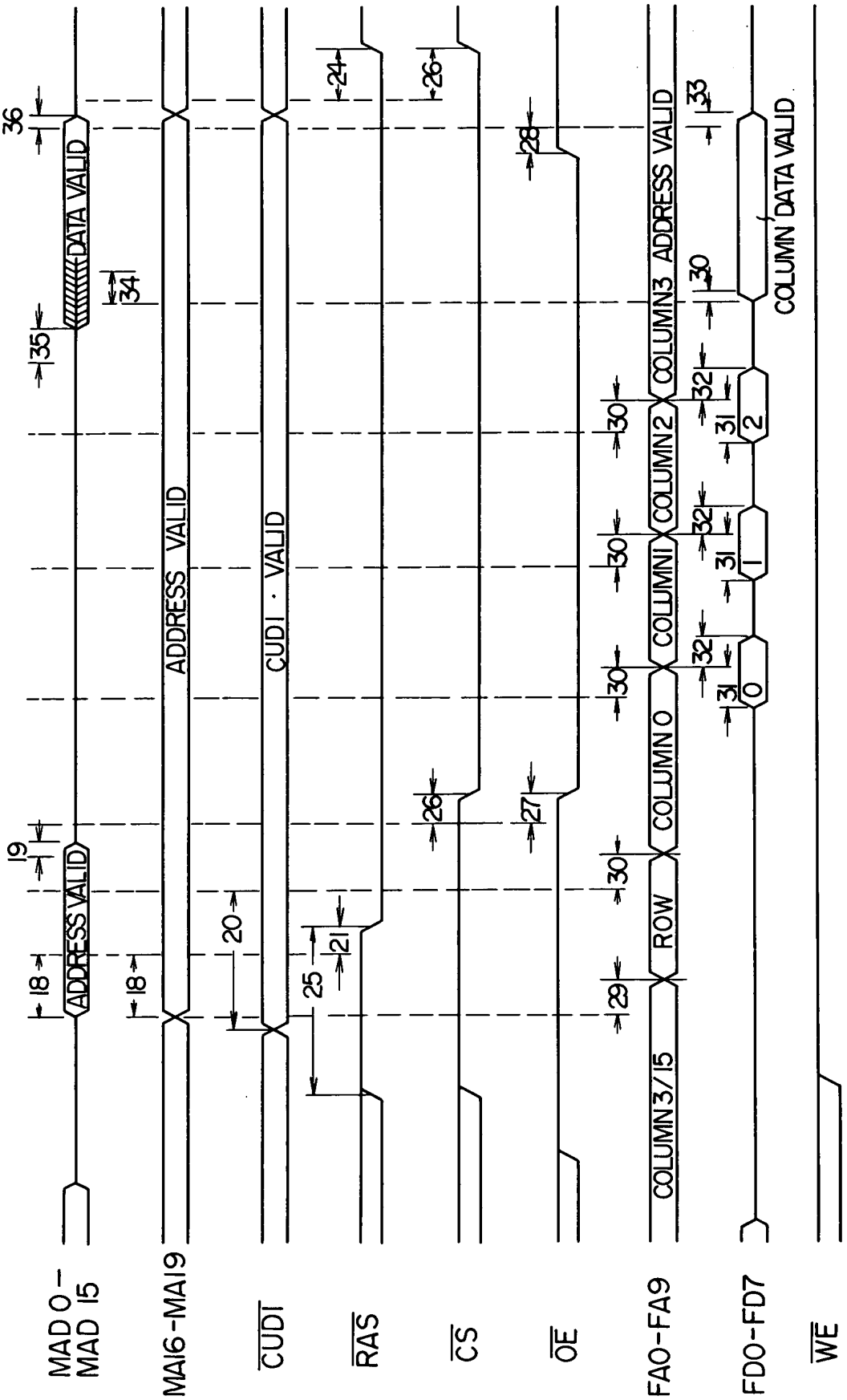


FIG. 15a

FIG. 15b



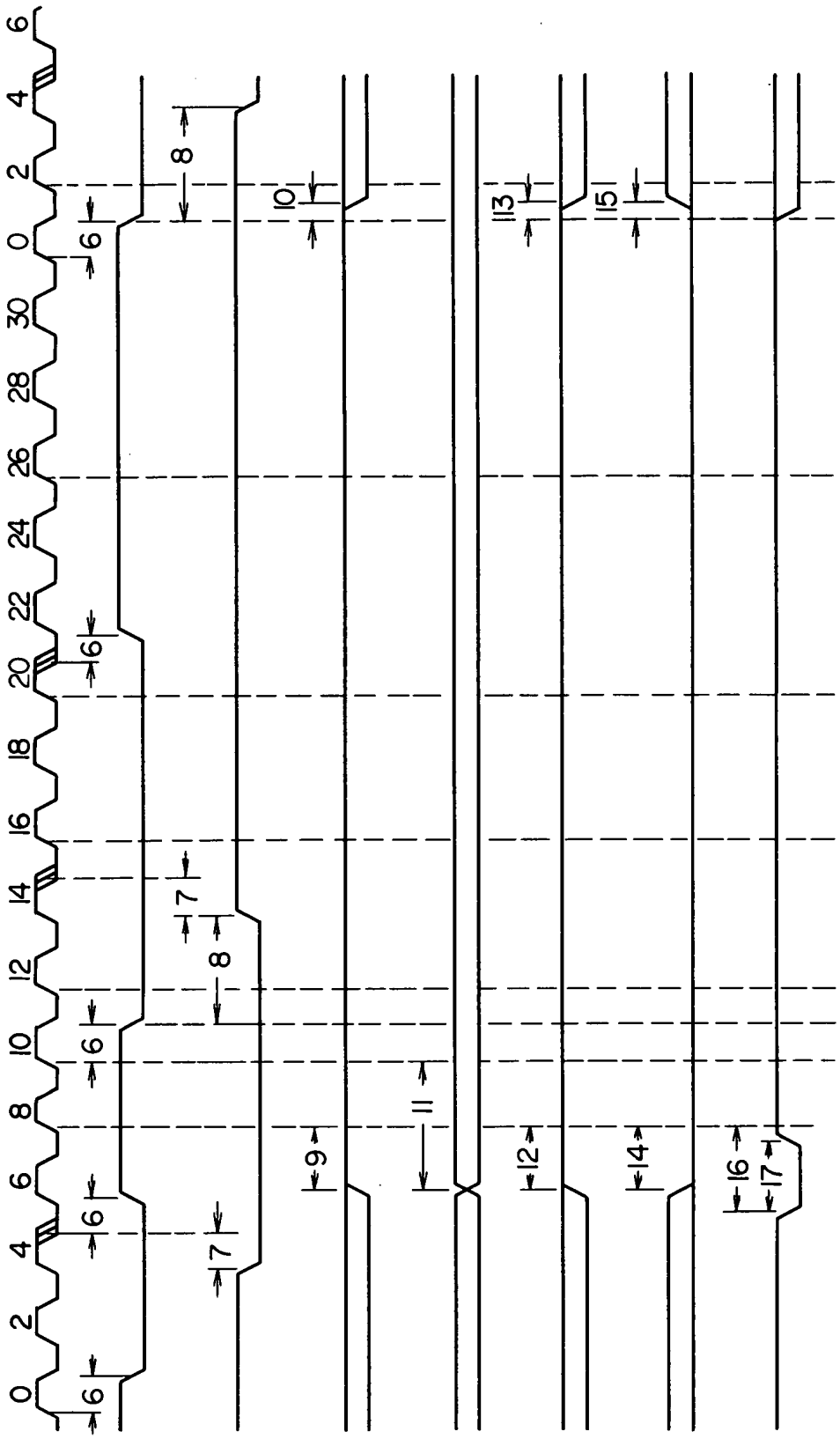


FIG. 16a

APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

FIG. 16b

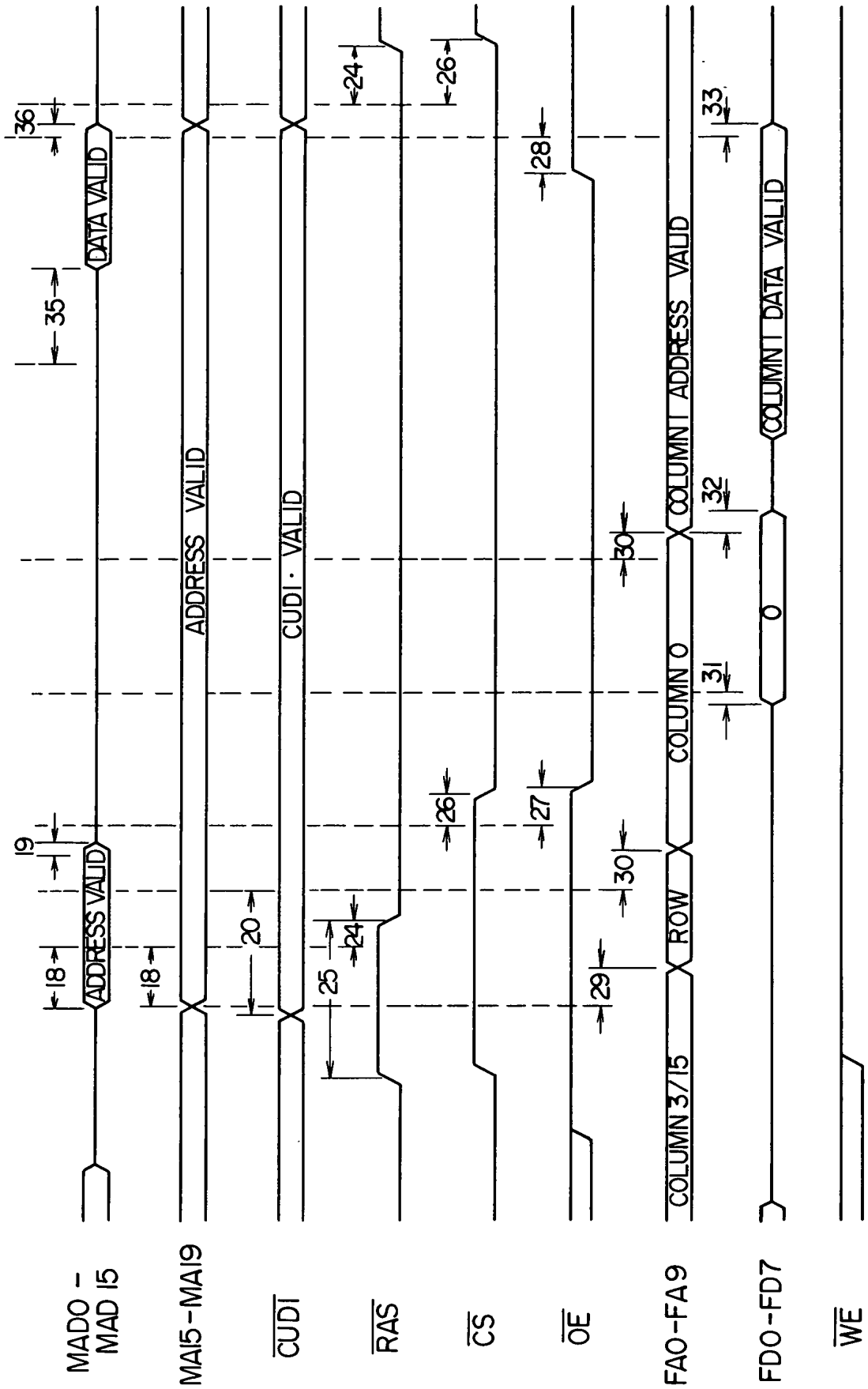
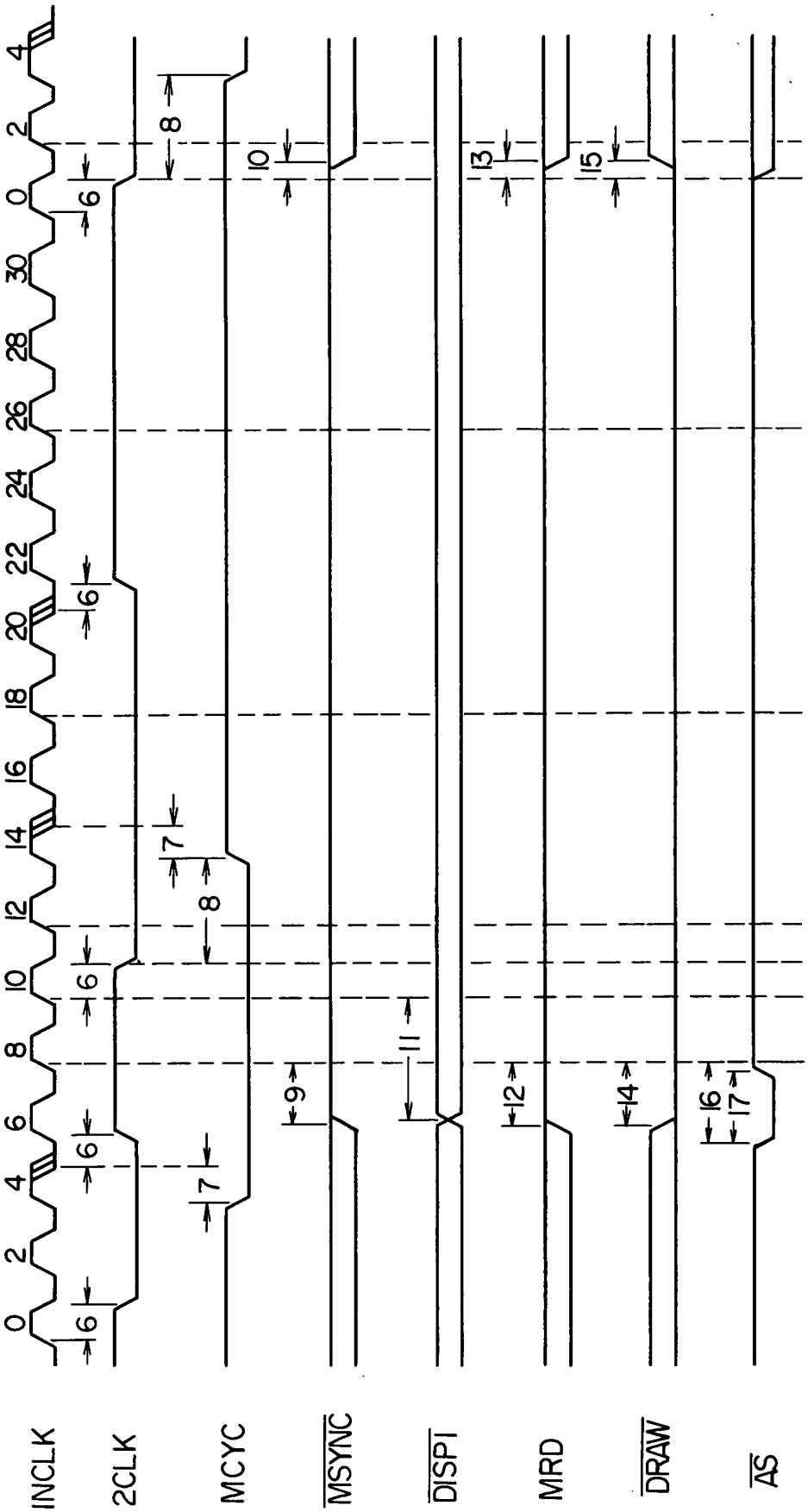
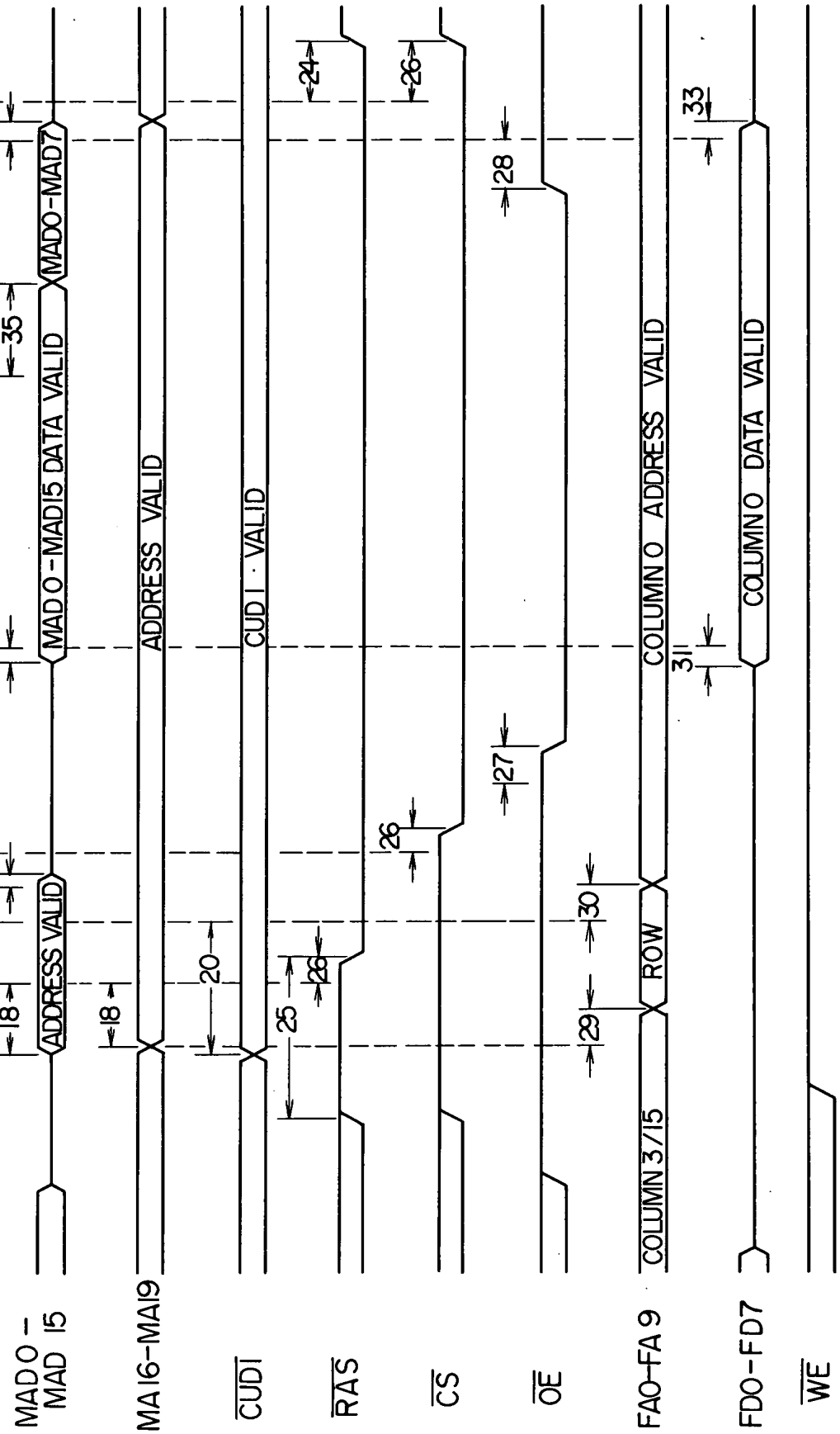


FIG. 17a



APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

FIG. 17b



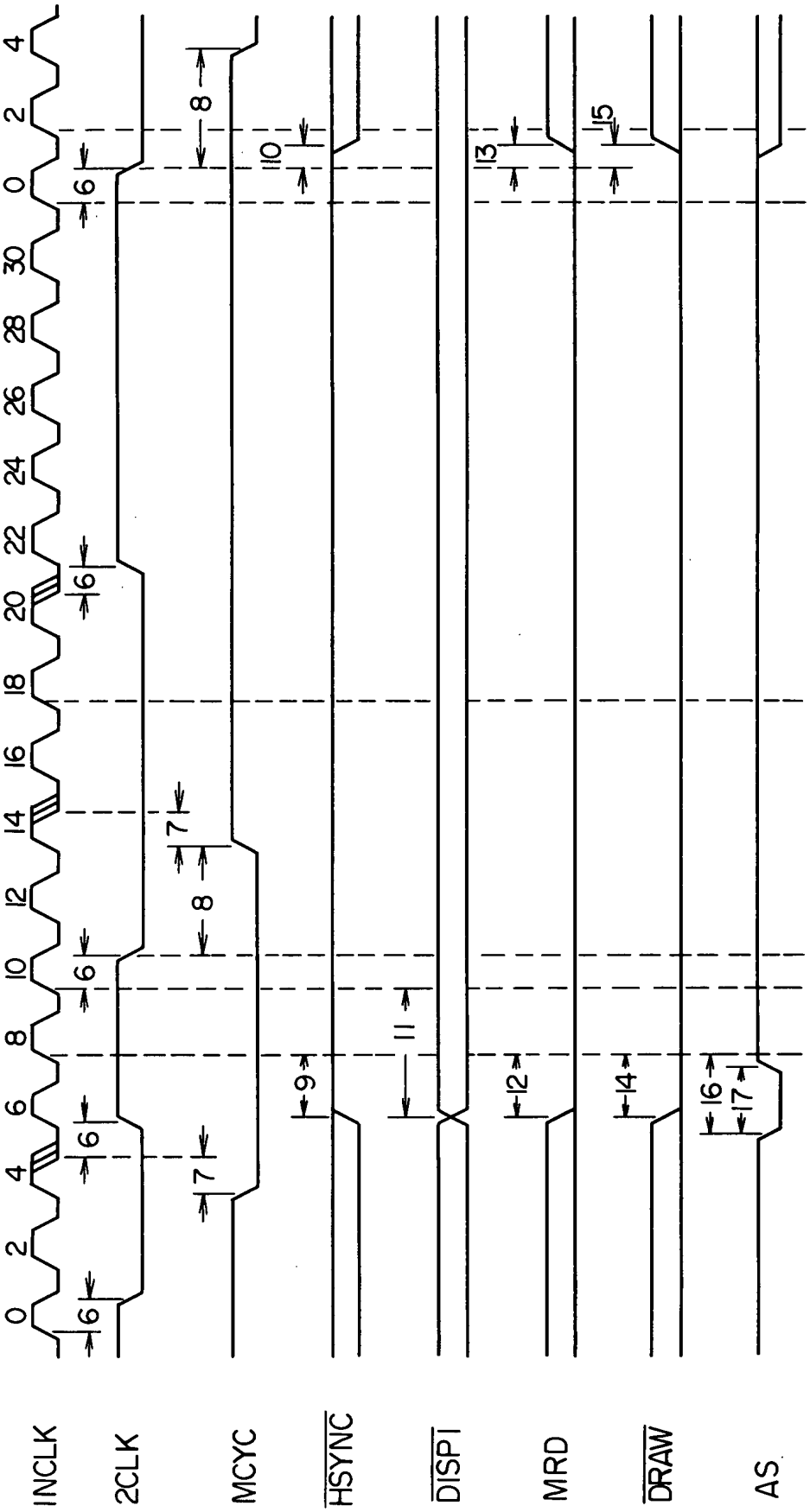
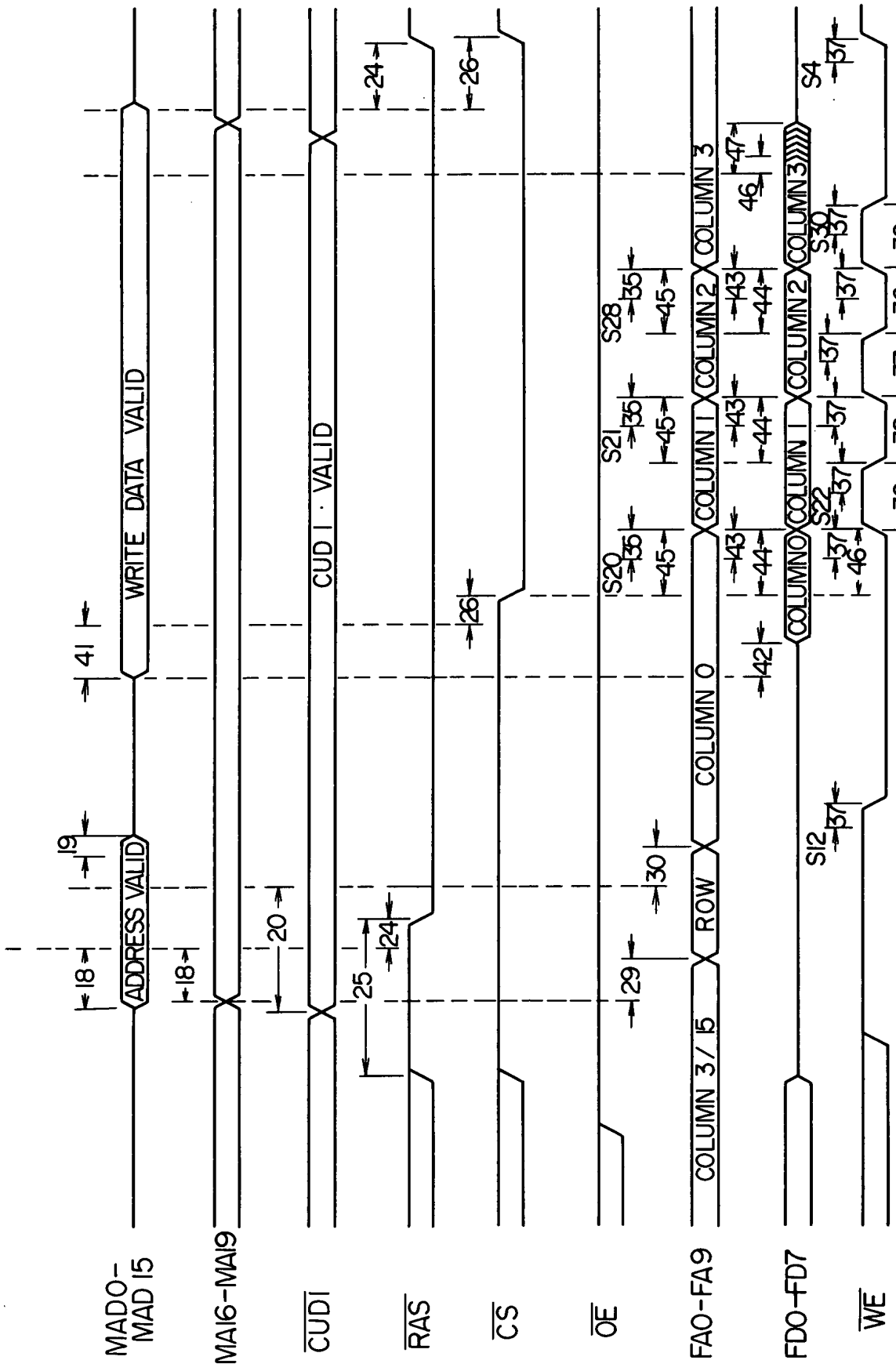


FIG. 18a

APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

FIG. 18b



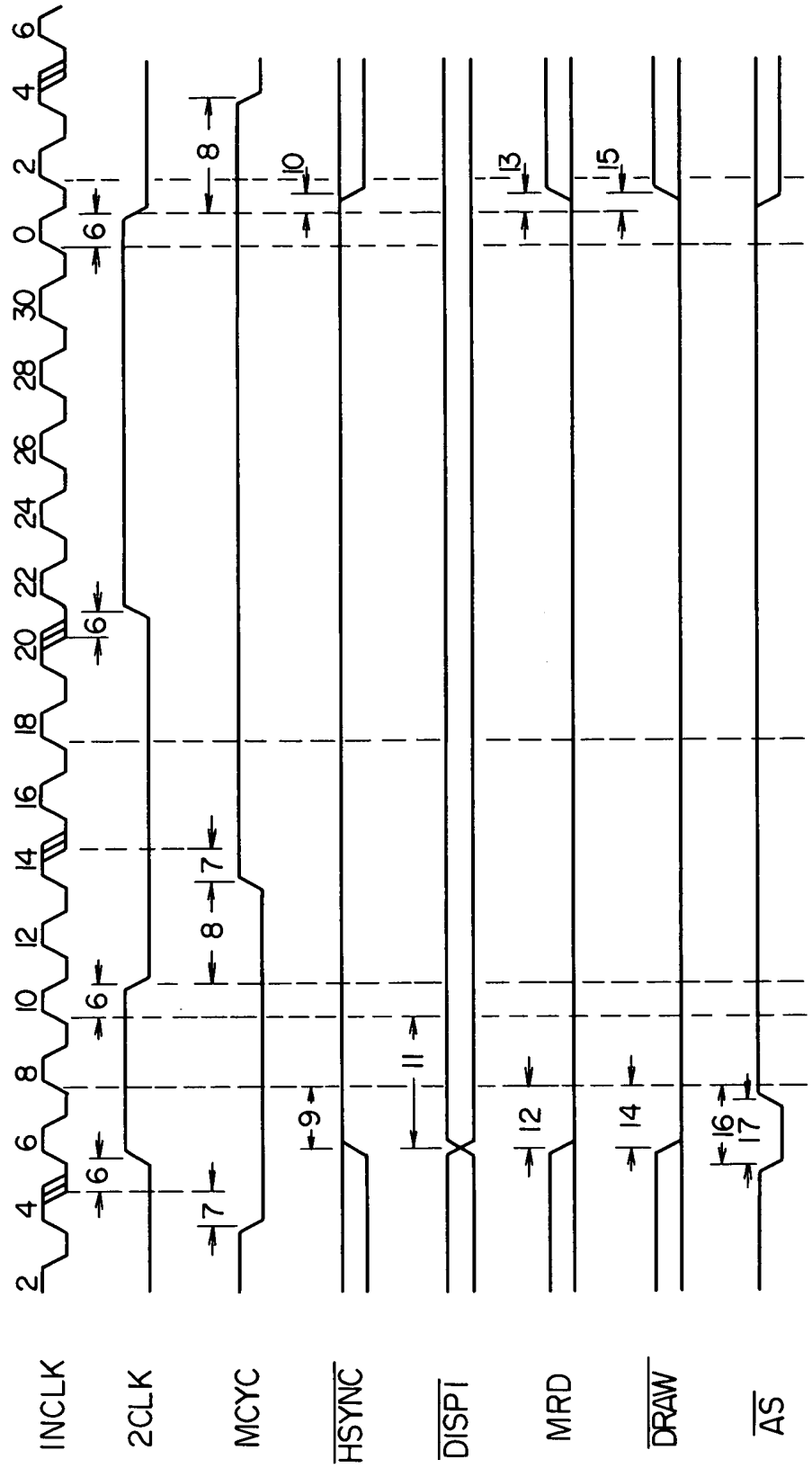


FIG. 19a

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 19b

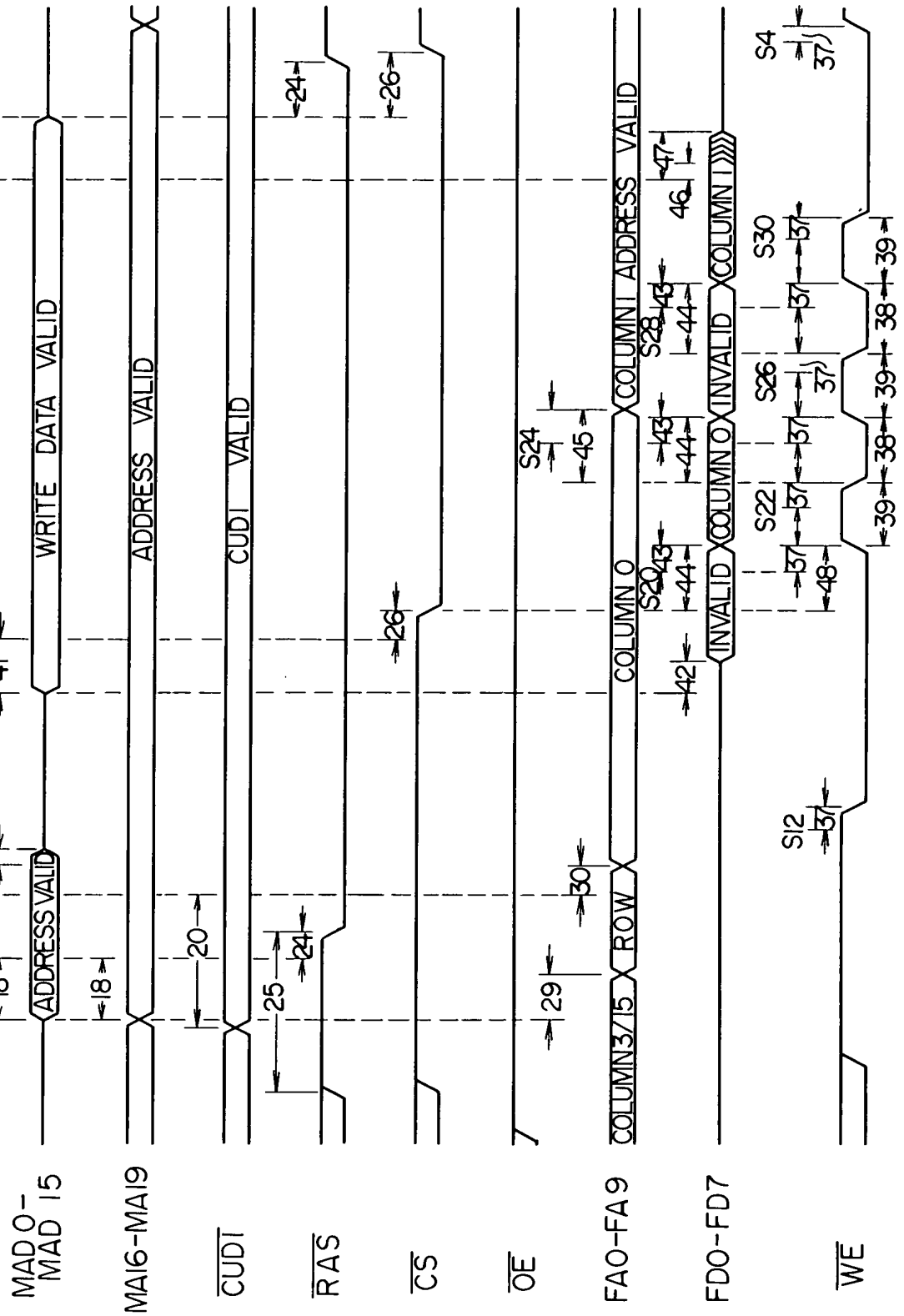
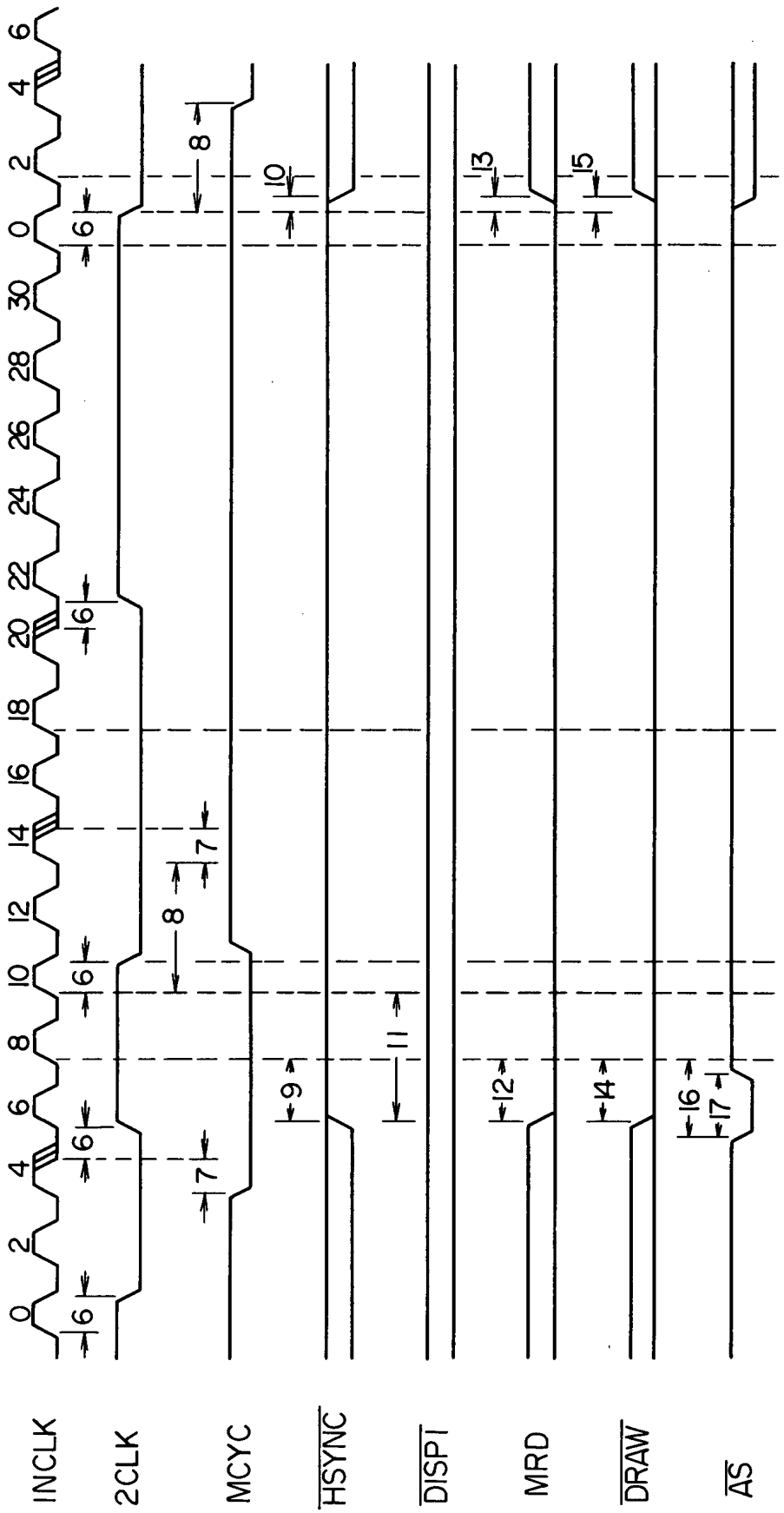
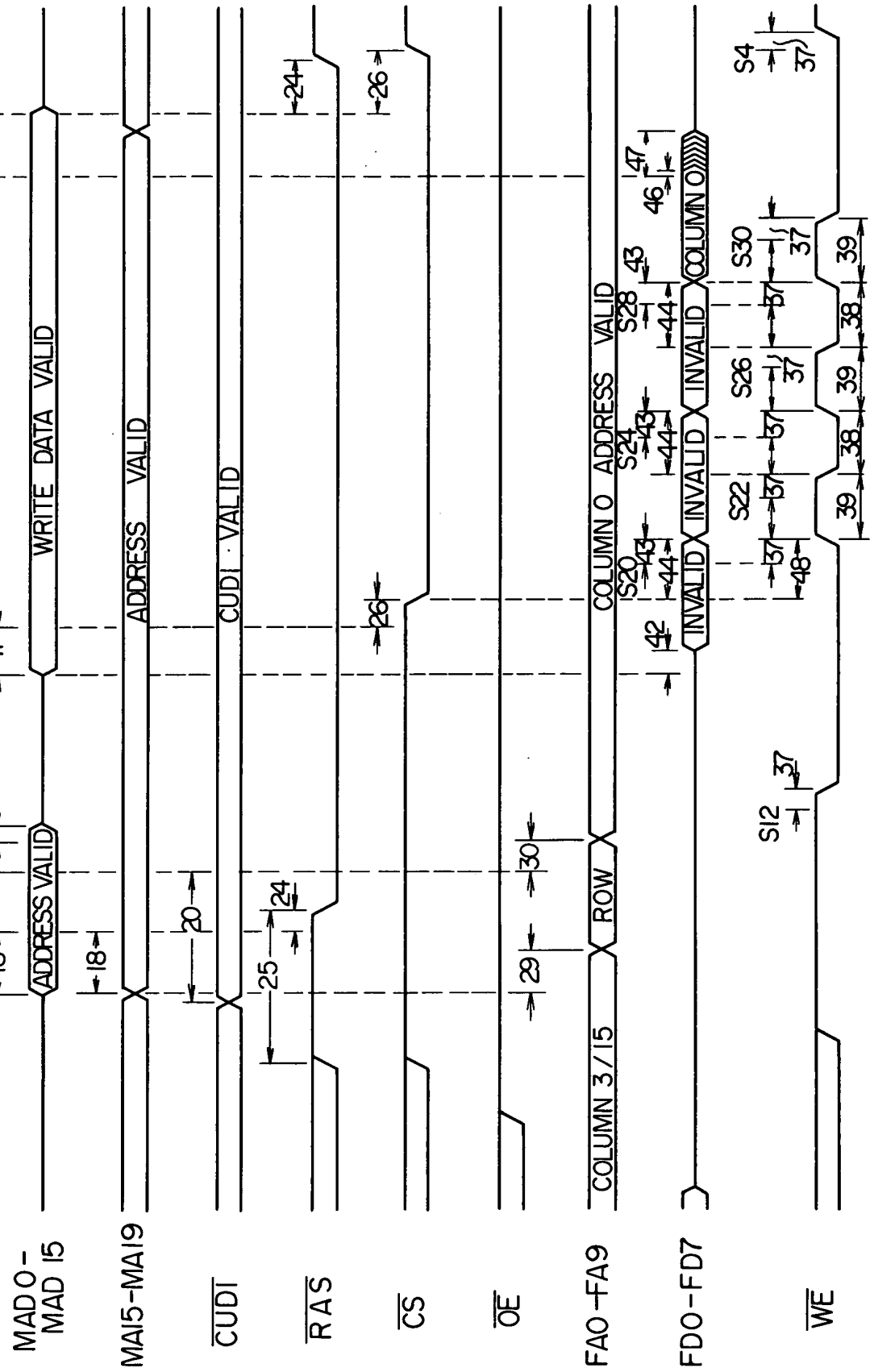


FIG. 20a



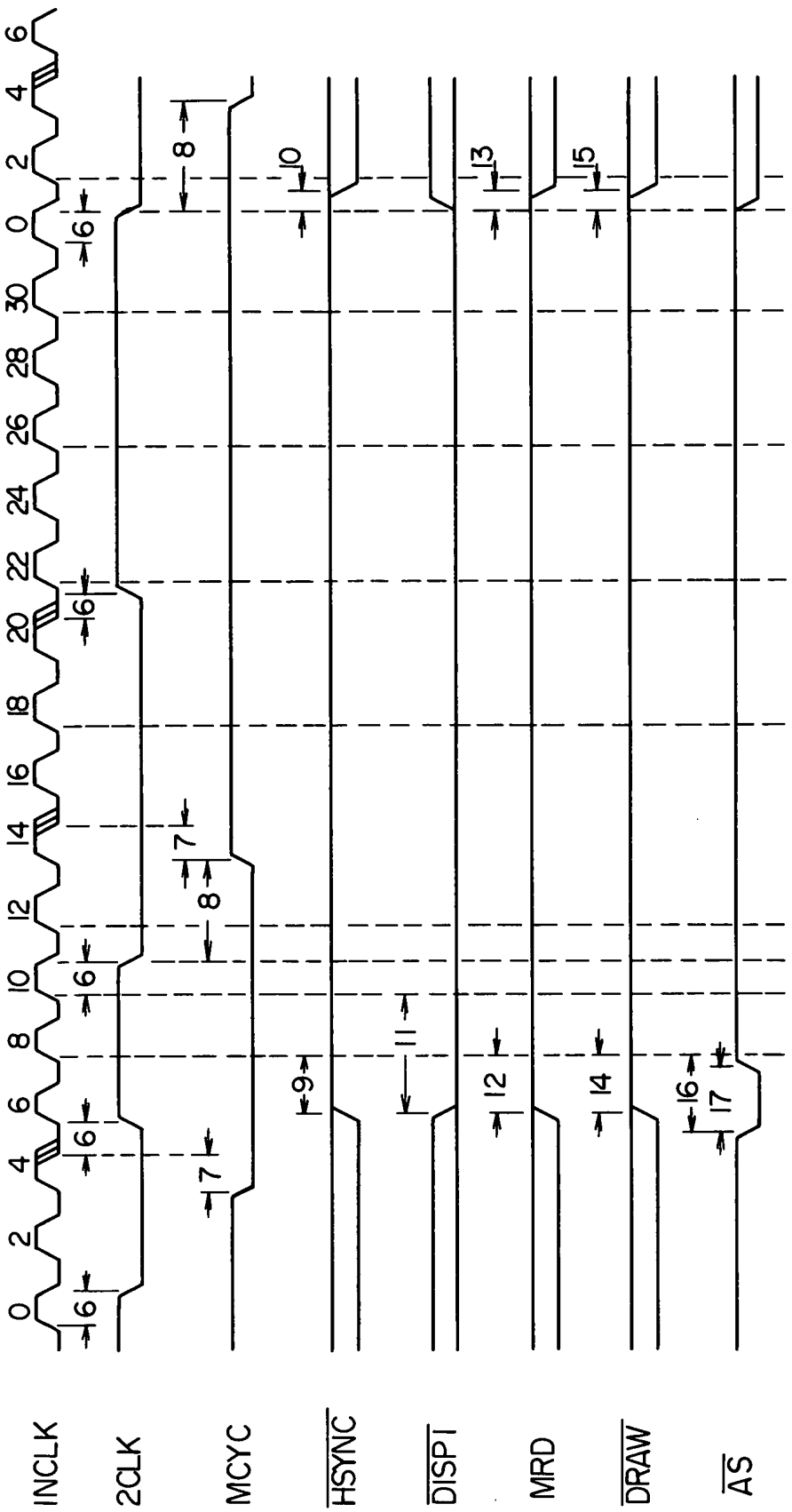
APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

FIG. 20b



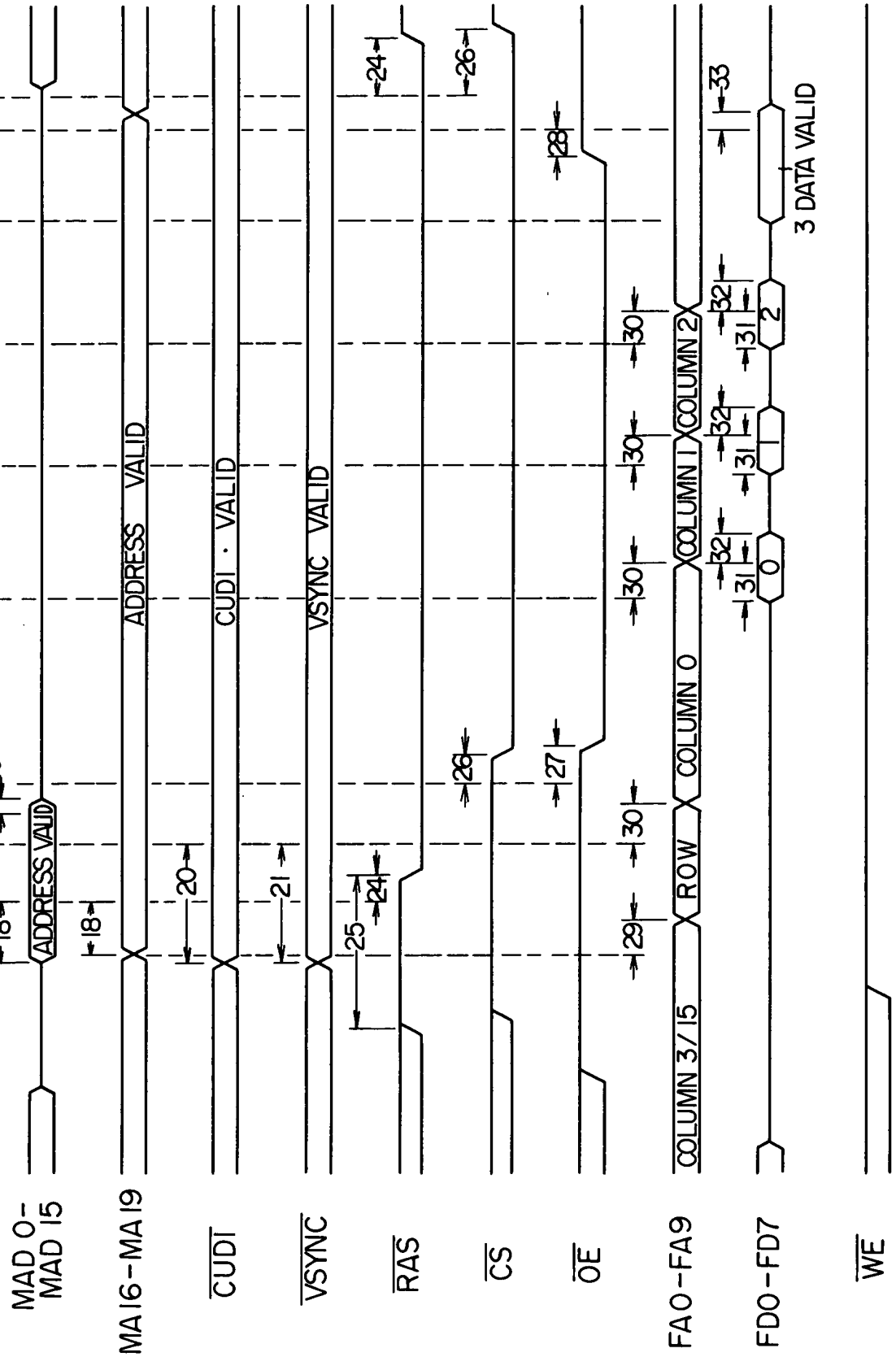
APPROVED BY DRAFTSMAN	O.G. FIG.	CLASS	SUBCLASS

FIG. 21a



APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

FIG. 21b



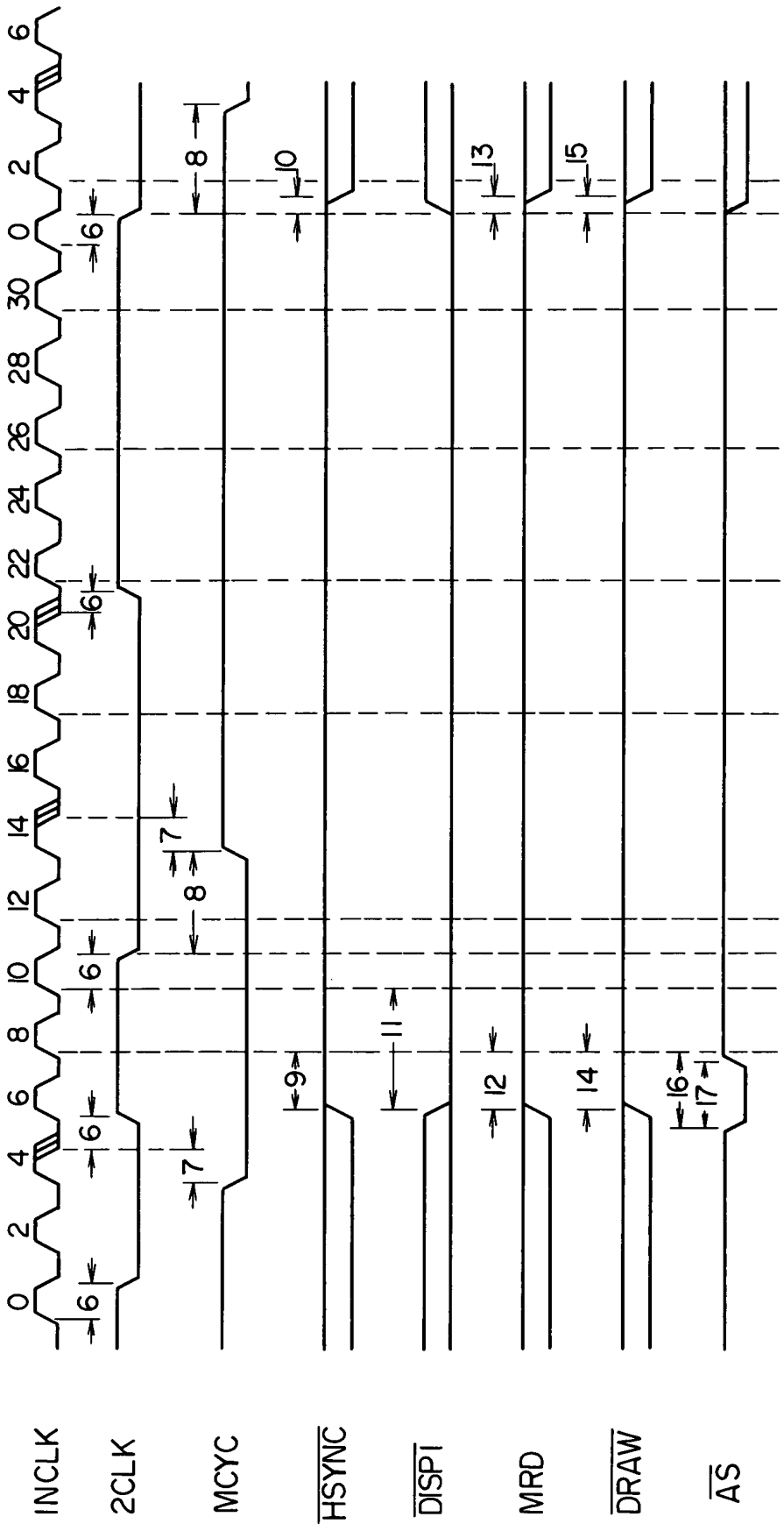
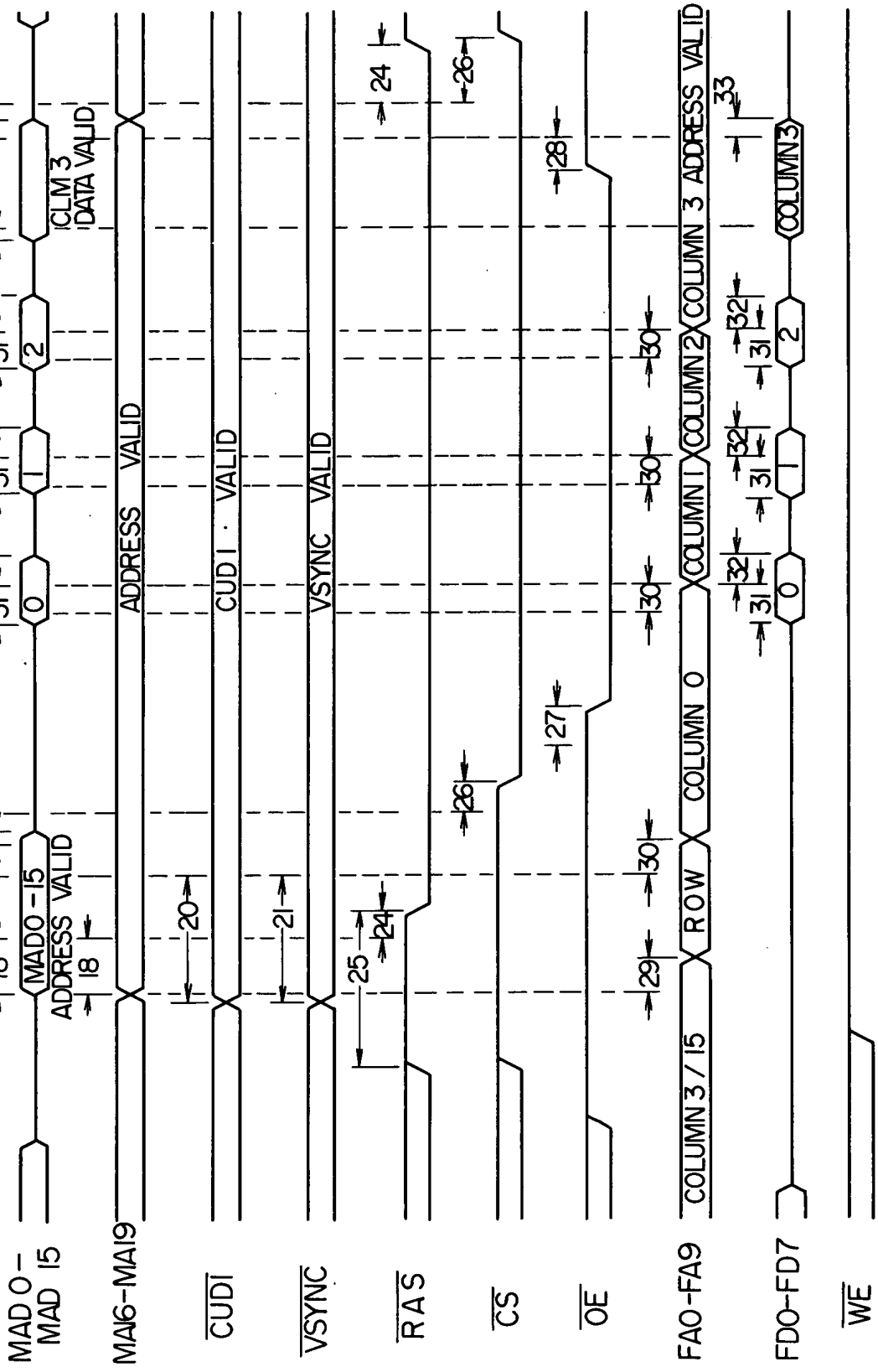


FIG. 22a

APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

FIG. 22b



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

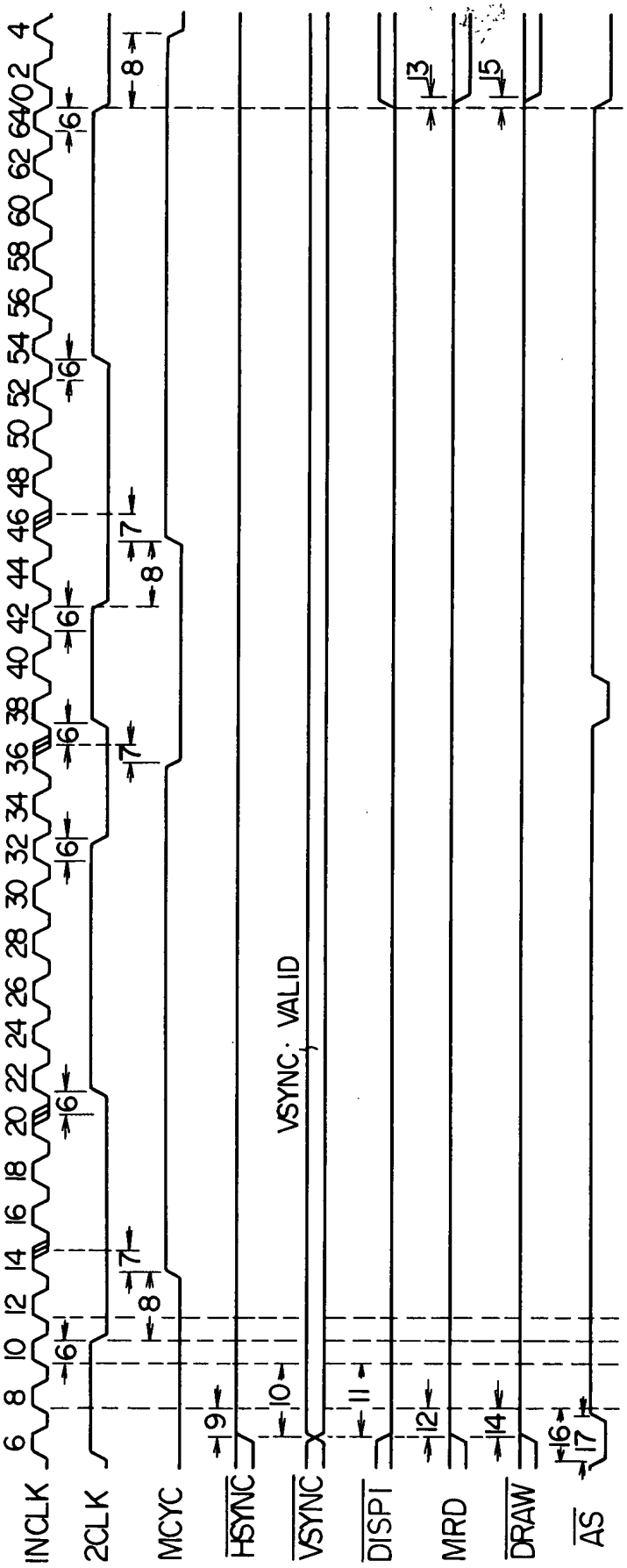
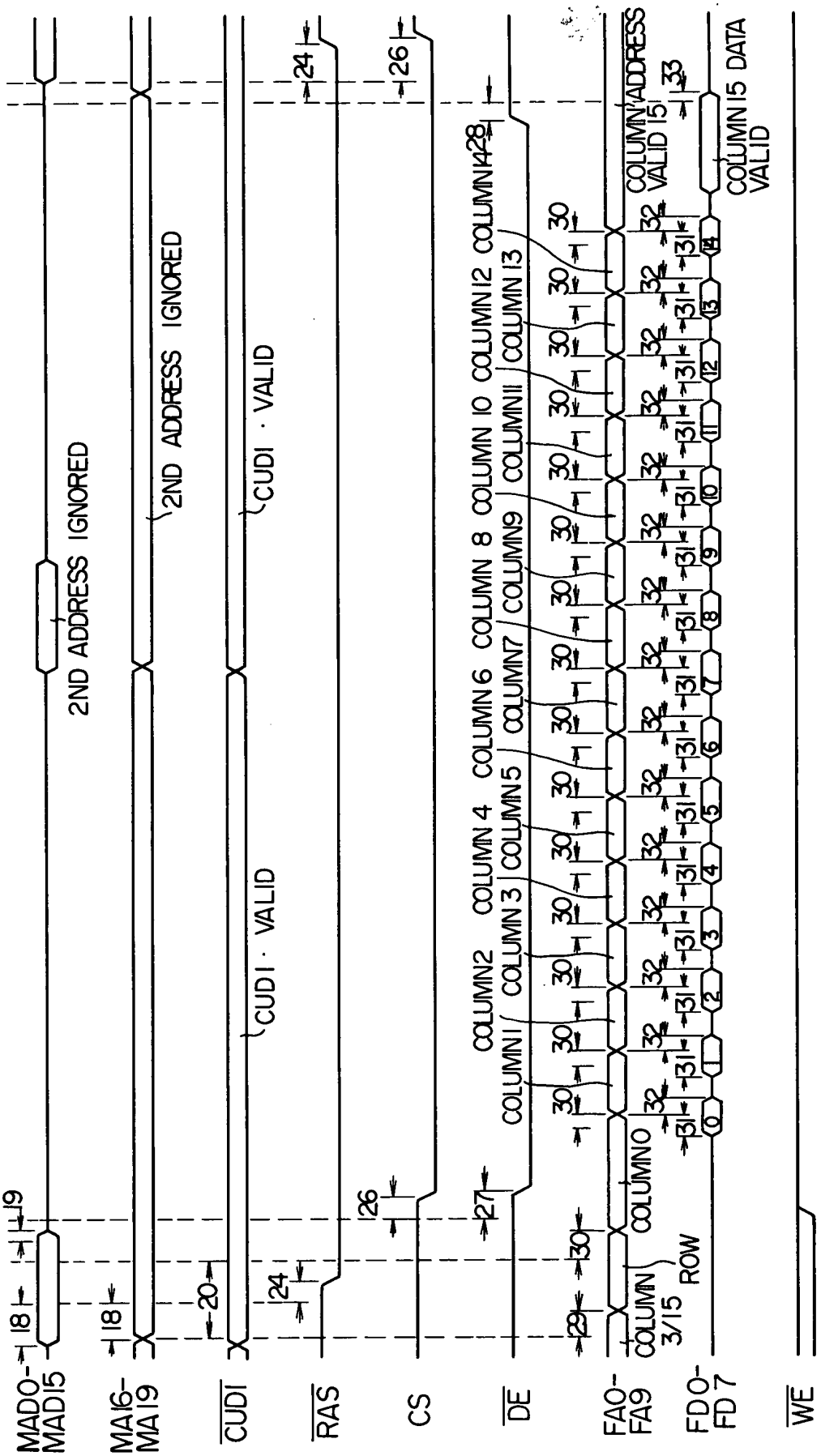


FIG. 23a

APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

FIG. 23b



APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

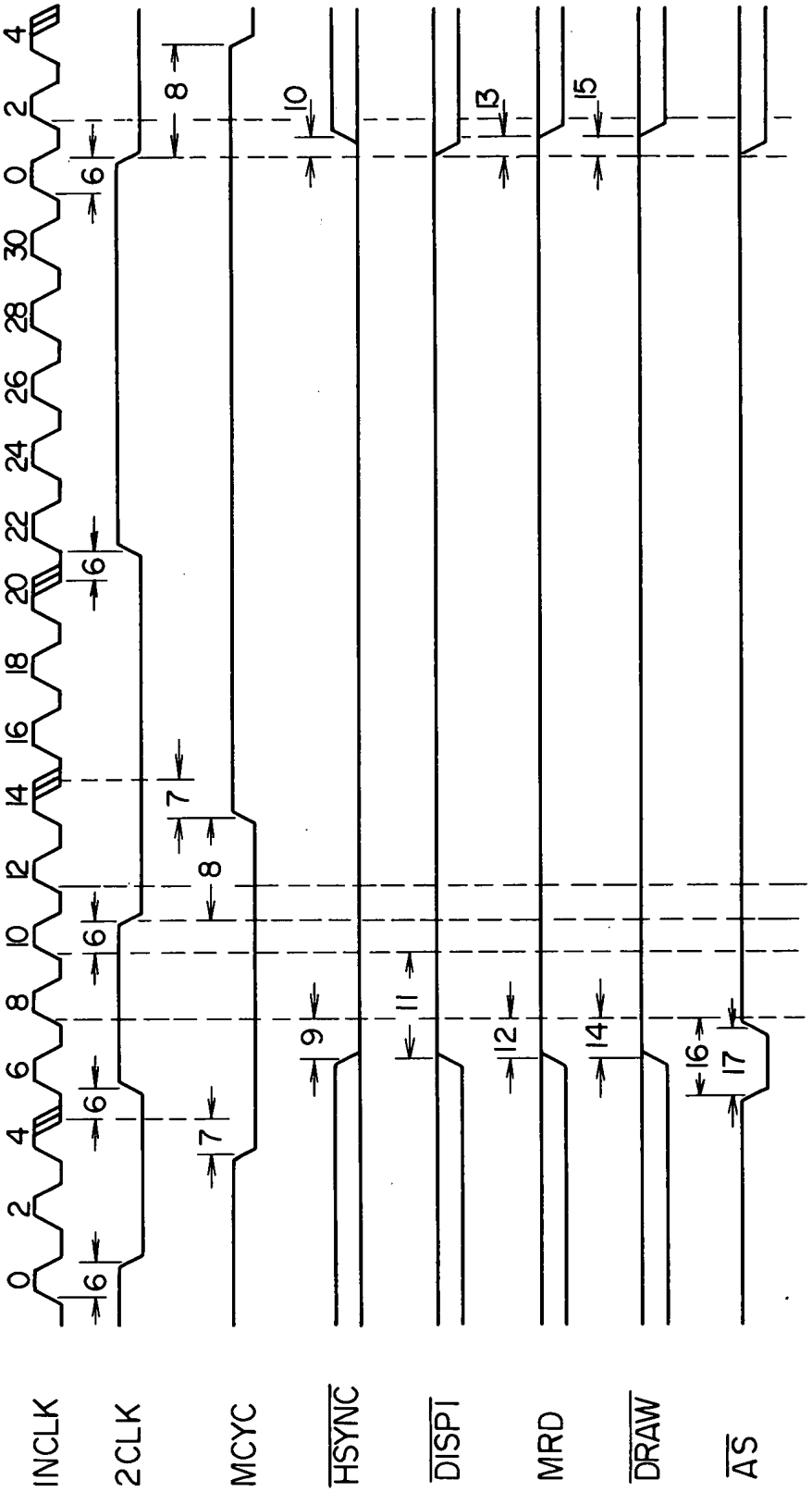


FIG. 24a

APPROVED BY DRAFTSMAN	O.G. FIG.	
	CLASS	SUBCLASS

FIG. 24b

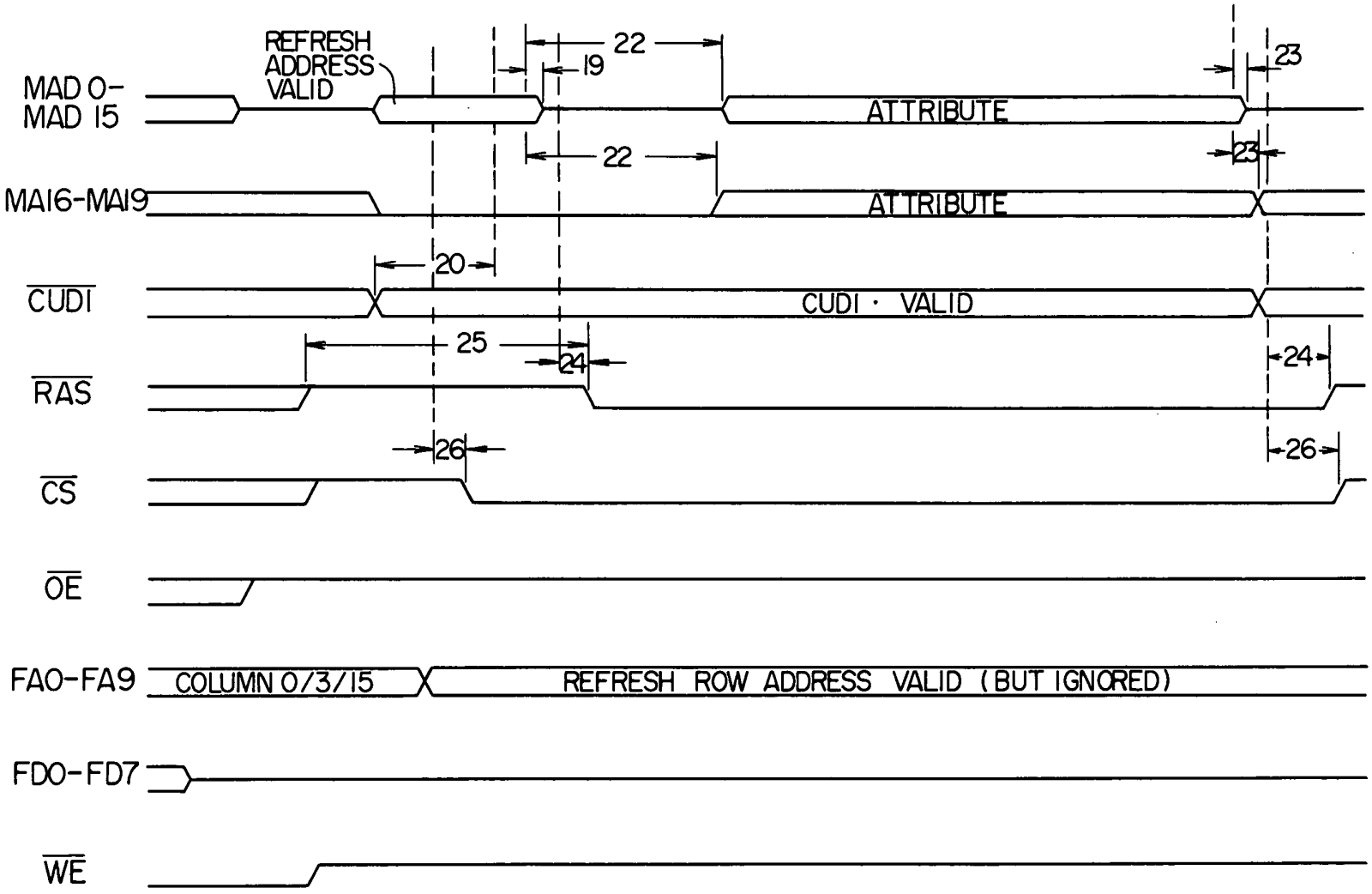


FIG. 25

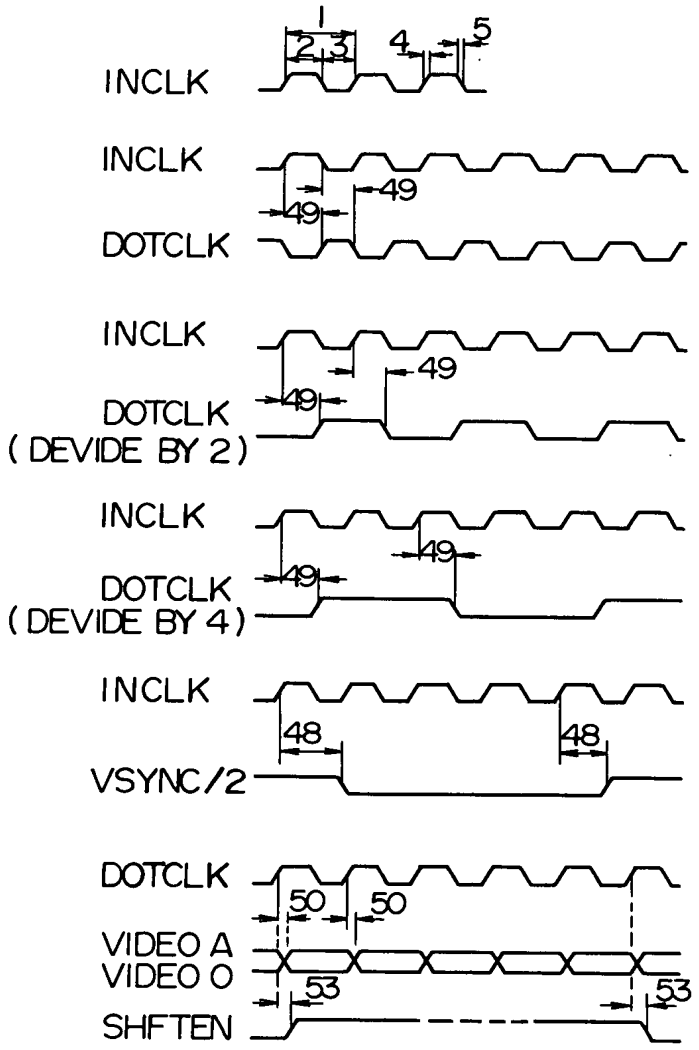
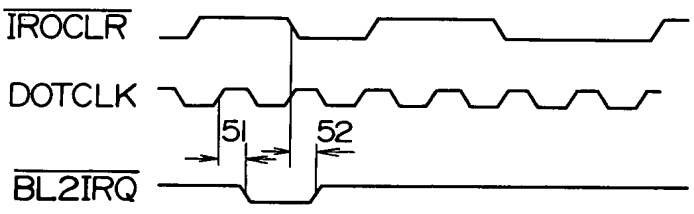


FIG. 26



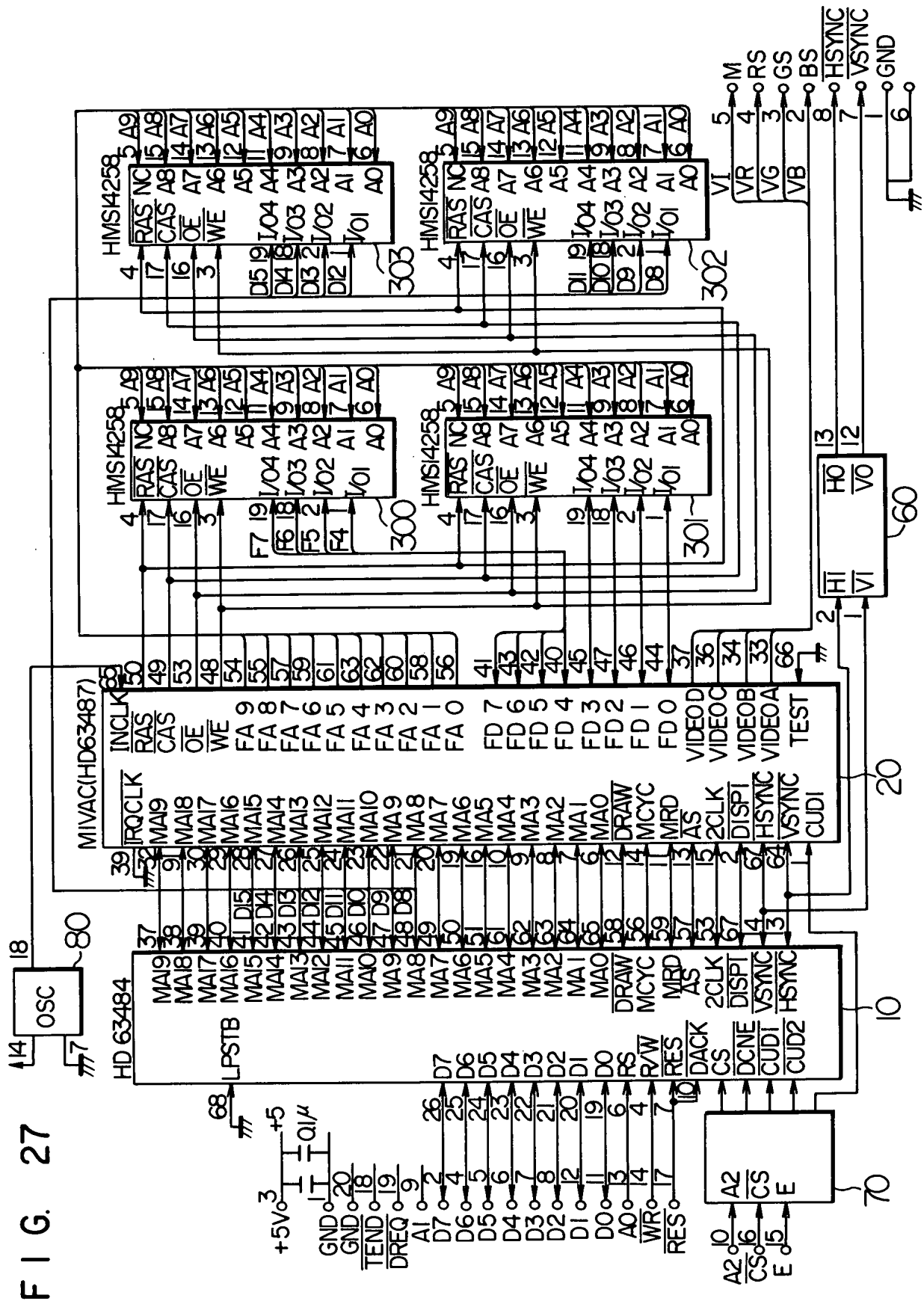


FIG. 27

FIG. 28

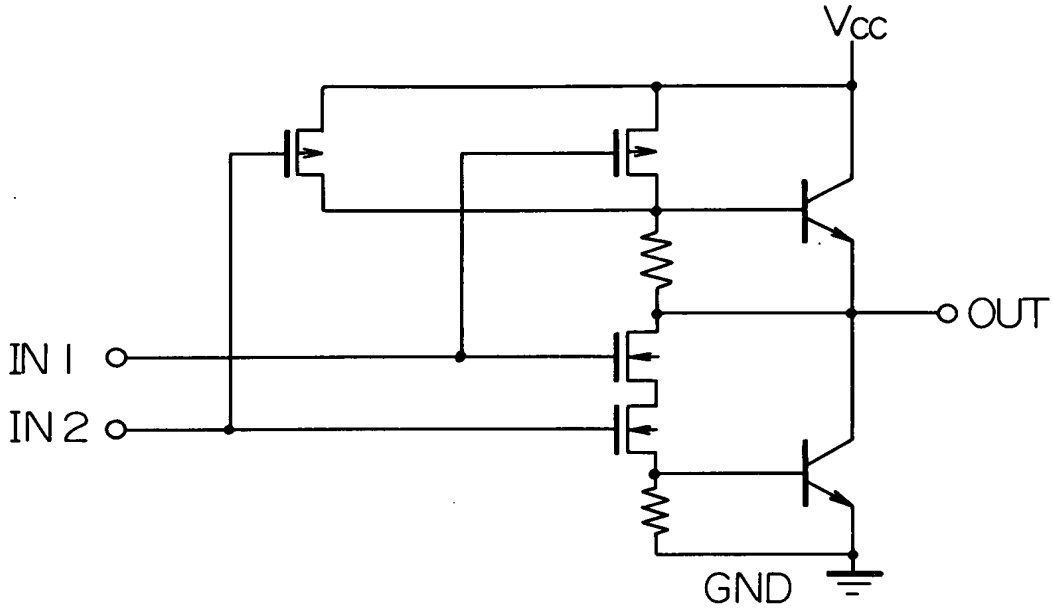


FIG. 29a

FA	4 ACCESSES / MCYC (DRAW, DISPLAY)				16 ACCESSES / 2 MCYCS (DISPLAY)			
	256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROM	COLUMN	ROM	COLUMN	ROM	COLUMN	ROM	COLUMN
9	—	—	MAD 8	NCO	—	—	MAD 8	NCO
8	MAD 9	NC 1	MAD 9	NC1	MAD 9	NC1	MAD 9	NC 1
7	MAD 8	NC 2	MA 17	MAD 7	MAD 8	NC2	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC 1	MAD 11	WC 1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC 0	MAD 10	WC 0

[ ] : COLUMN ADDRESS COUNTER

F I G. 29b

FA	2 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)				16 ACCESSES / 2MCYCS (DISPLAY)			
	256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	–	–	MA 18	[NC 0]	–	–	MA 18	[NC 0]	–	–	MA 18	[NC 0]
8	MAD 9	[NC 1]	MAD 9	MAD 8	MAD 9	[NC 1]	MAD 9	MAD 8	MAD 9	[NC 1]	MAD 9	MAD 8
7	MAD 8	MAD 7	MA 17	MAD 7	MAD 8	MAD7	MA 17	MAD 7	MAD 8	MAD 7	MA 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 14
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	[WC 2]	MAD 12	[WC 2]
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	[WC 1]	MAD 11	[WC 1]
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	[WC 0]	MAD 10	[WC 0]	MAD 10	[WC 0]	MAD 10	[WC 0]

[ ] : COLUMN ADDRESS COUNTER

FIG. 29c

FA	1 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)			
	256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	–	–	MA 18	MAD 9	–	–	MA 18	MAD 9
8	MAD 9	MAD 8	MA 19	MAD 8	MAD 9	MAD 8	MA 19	MAD 8
7	MA 17	MAD 7	MA 17	MAD 7	MA 17	MAD 7	MAD17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC0	MAD 10	WC0

[ ]: COLUMN ADDRESS COUNTER